Exhibit C to the
Supplemental Declaration of Dr. Richard Blanchard
(declaration filed under seal)

T5761/T5761ES

Memory Test System

Parallel Test for up to 512 NAND Flash Memory Devices

T5761

T5761ES

Demand for NAND flash memory continues to rise dramatically, propelled by an insatiable demand for consumer gadgetry, including computerized devices, cellular telephones, portable music players, digital video appliances, and car navigation systems. And, the geometric bit growth and multi level cell technology in data flash drives longer test times while the consumer market drives a commodity price point, demanding further reductions in the overall cost of test. The T5761 memory test system answers these calls with significant reductions in test time, and with its 512-device parallel test capability, per-site architecture, Error Code Correction (ECC), and real-time test programming functionality, the system also affords greatly reduced test costs.

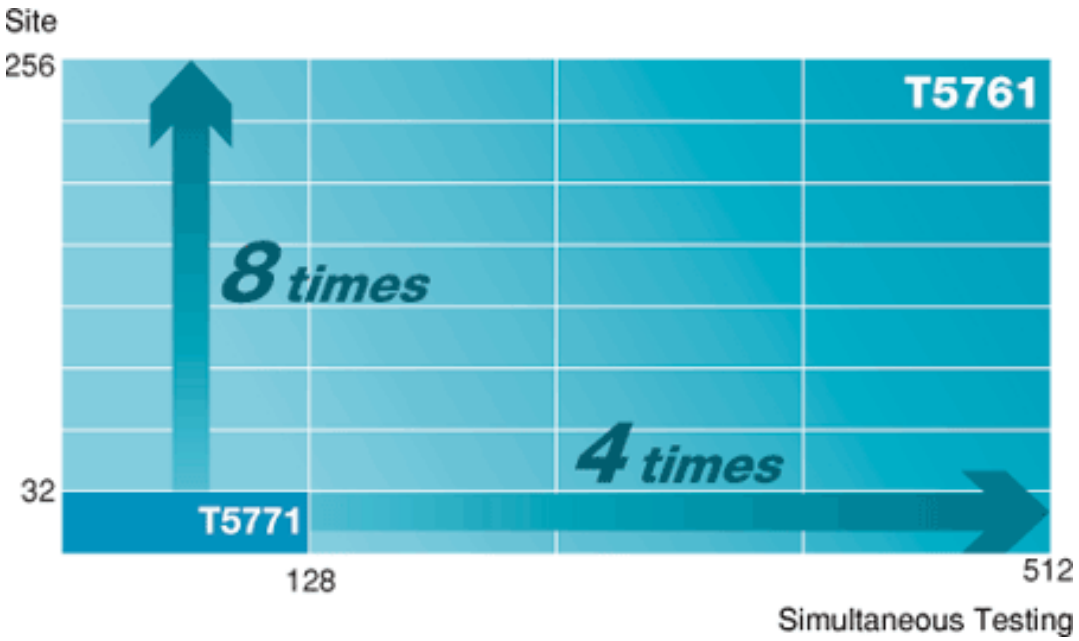
Improving throughput with 512-device parallel test and ECC
With its per-site architecture, which allows testing of 2 DUTs NAND flash memories in parallel within a site, the T5761 provides the capability to parallel-test up to 512 devices. As a result, test can be performed independently for each device, and at a high rate of throughput. This model's support for ECC, a device feature previously difficult to support without significant test time impact , provides for shorter test times, along with significantly improved yields. Real time ECC support is a must for the shrinking geometry and bit density of newer NAND Flash..

A compact engineering station

The T5761ES (Engineering Station) brings cost reduction capabilities to test program development and evaluation of small quantities of devices.
The T5761ES offers the performance and functionality of the T5761, but within a compact form factor. With this engineering station, device evaluation and the deployment of test programs into volume-production is now simplified.

Using FutureSuite®, with multi-language support

FutureSuite allows program development and evaluation/analysis making maximal use of per-site architecture. It delivers full coverage extending from the design stage through volume production. Also, FutureSuite, with its multi-language support, enables the user to program either in the C-based MCI (multi control interface) language or in ATL, providing a compatible syntax to the industry's most common memory platforms.



Major Specifications

Model Number:	T5761	T5761ES
Target Devices:	FLASH memory, EPROM, etc.	
Simultaneous Testing:	Up to 512 devices	Up to 16 devices
Test speed:	66 MHz	

Products

19-0474; Rev 0; 6/06

MAXIM

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

General Description

The MAX9971/MAX9972 four-channel, ultra-low-power, pin-electronics ICs include, for each channel, a three-level pin driver, a window comparator, a passive load, and force-and-sense Kelvin-switched parametric measurement unit (PMU) connections. The driver features a -2.2V to +5.2V voltage range, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The window comparator features 500MHz equivalent input bandwidth and programmable output voltage levels. The passive load provides pullup and pulldown voltages to the device-under-test (DUT).

Two grade versions are available, A grade and B grade. The A-grade version provides tight gain and offset matching for the driver and comparator, allowing reference levels to be shared across multiple channels. It also provides tighter tolerance of the load resistance values. The B-grade version is for system designs that incorporate independent reference levels for each channel.

Low-leakage, high-impedance, and terminate controls are operational configurations that are programmed through a 3-wire, low-voltage, CMOS-compatible serial interface. High-speed PMU switching is realized through dedicated digital control inputs.

These devices are available in an 80-pin, 12mm x 12mm body, 1.0mm pitch TQFP with an exposed 6mm x 6mm die pad on the bottom of the package (MAX9972), and the top of the package (MAX9971), for efficient heat removal. The MAX9971/MAX9972 are specified to operate over the 0°C to +70°C commercial temperature range, and feature a die temperature monitor output.

Applications

NAND Flash Testers

DRAM Probe Testers

Low-Cost Mixed-Signal/System-on-Chip (SOC) Testers

Active Burn-In Systems

Structural Testers

Features

- ♦ **Small Footprint—Four Channels in 0.3in²**
- ♦ **Low-Power Dissipation: 325mW/Channel Typical**
- ♦ **High Speed: 300Mbps at $3V_{P-P}$**
- ♦ **-2.2V to +5.2V Operating Range**
- ♦ **Active Termination (3rd-Level Drive)**
- ♦ **Integrated PMU Switches**
- ♦ **Passive Load**
- ♦ **Low-Leak Mode: 20nA max**
- ♦ **Low Gain and Offset Error**
- ♦ **Lead-Free Package Available**

Pin Configurations appear at end of data sheet.

Ordering Information and Selector Guide

PART	ACCURACY GRADE	PIN-PACKAGE	PKG CODE	HEAT EXTRACTION
MAX9971ACCS*	A	80 TQFP-IDP†	—	Top
MAX9971BCCS*	B	80 TQFP-IDP†	—	Top
MAX9972ACCS*	A	80 TQFP-EP††	C80E-4	Bottom
MAX9972BCCS	B	80 TQFP-EP††	C80E-4	Bottom

**Future product—contact factory for availability.*

Note: *All devices are specified over the 0°C to +70°C operating temperature range.*

All versions available in both leaded and lead-free packaging. Specify lead-free by adding the "+" symbol at the end of the part number when ordering.

†*IDP = Inverted die pad.*

††*EP = Exposed paddle.*

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +9.4V
V_{SS} to GND .....-6.25V to +0.3V
V_{DD} to V_{SS} .....+15.7V
V_L to GND .....-0.3V to +5V
V_{DD} to GND .....-0.3V to +9.4V
DHV_, DTV_, DLV_, DATA_, RCV_, LDV_, DUT_ to GND .....V_{SS} to V_{DD}
CHV_, CLV_, CMPH_, CMPL_, COMPHI, COMPLO to GND .....V_{SS} to V_{DD}
FORCE_, SENSE_, PMU_ to GND .....V_{SS} to V_{DD}
$\overline{LD}$, DIN, SCLK, $\overline{CS}$ to GND .....-0.3V to +5V
DUT_, CMPH_, CMPL_ Short-Circuit Duration .....Continuous
DHV_, DLV_, DTV_ to Each Other .....V_{SS} to V_{DD}
CHV_, CLV_ to DUT_ .....V_{SS} to V_{DD}
DOUT to GND .....-0.3V to +5V
TEMP Short-Circuit Duration .....Continuous
Continuous Power Dissipation (T_A = +70°C)
80-Pin TQFP-EP (derate 35.7mW/°C above +70°C) 2857mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER (all specifications apply when DUT_ = DHV_, DUT_ = DTV_, or DUT_ = DLV_)							
DC CHARACTERISTICS							
Voltage Range				-2.2		+5.2	V
Gain		Measured at 0 and 3V	A grade	0.995	1	1.005	V/V
			B grade	0.95		1.05	
Gain Temperature Coefficient					50		ppm/°C
Offset		$V_{DHV\_}$ = 2V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1V	A grade			±7	mV
			B grade			±100	
Offset Temperature Coefficient					±250		µV/°C
Power-Supply Rejection Ratio	PSRR	V_{DD}, V_{SS} independently varied over full range				18	mV/V
Maximum DC Drive Current	$I_{DUT\_}$			±40		±90	mA
DC Output Resistance		$I_{DUT\_}$ = ±10mA (Note 2)		48.5	49.5	50.5	Ω
DC Output Resistance Variation		$I_{DUT\_}$ = -40mA to +40mA				2.5	Ω
DC Crosstalk		DHV to DLV and DTV: $V_{DLV\_}$ = $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -2.2V, +5.2V				5	mV
		DLV to DHV and DTV: $V_{DHV\_}$ = $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -2.2V, +5.2V				5	
		DTV to DHV and DLV: $V_{DHV\_}$ = $V_{DLV\_}$ = +1.5V, $V_{DTV\_}$ = -2.2V, +5.2V				5	
Linearity Error		0 to 3V (Note 3)				±5	mV
		Full range (Note 4)				±15	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (Note 5)						
Dynamic Output Current		(Note 1)	40			mA
Drive-Mode Overshoot, Undershoot, and Preshoot		200mV to 4V_{P-P} swing (Note 6)		5% +10		mV
Term-Mode Spike		$V_{DHV\_}$ = $V_{DTV\_}$ = 1V, $V_{DLV\_}$ = 0		25		mV
		$V_{DLV\_}$ = $V_{DTV\_}$ = 0, $V_{DHV\_}$ = 1V		25		
High-Impedance-Mode Spike		$V_{DLV\_}$ = -1.0V, $V_{DHV\_}$ = 0		25		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		25		
Prop Delay, Data to Output				2		ns
Prop-Delay Temperature Coefficient				10		ps/°C
Prop-Delay Match, t_{LH} vs. t_{HL}				30		ps
Prop-Delay Skew, Drivers Within Package				150		ps
Prop-Delay Change vs. Pulse Width		Relative to 12.5ns pulse, 3V_{P-P}, 40MHz, PW = 4ns to 21ns		20		ps
		Relative to 12.5ns pulse, 1V_{P-P}, 40MHz, PW = 2.5ns to 23.5ns		90		
Prop-Delay Change vs. Common-Mode Voltage		1V_{P-P}, $V_{DLV\_}$ = 0 to 3V, relative to delay at $V_{DLV\_}$ = 1V		80		ps
Prop Delay, Data to High Impedance		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V, both directions		1.8		ns
Prop Delay, Data to Term		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 0, both directions		1.6		ns
Minimum Voltage Swing		(Note 7)		25		mV
Rise/Fall Time		$V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0, 20% to 80%		0.7		ns
		$V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0, 20% to 80%		0.7		
		$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 10% to 90%	1.5	2.0	2.5	
		$V_{DHV\_}$ = 4V, $V_{DLV\_}$ = 0, R_L = 500Ω, 10% to 90%		2.6		
		$V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0, R_L = 500Ω, 10% to 90%		3.4		
Rise/Fall-Time Matching		$V_{DHV\_}$ = 1V to 5V		±5		%
Minimum Pulse Width (Note 8)		200mV, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0		1.8		ns
		1V, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0		2.4		
		3V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0		3.3		

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR (Note 9)							
DC CHARACTERISTICS (driver in high-impedance mode)							
Input Voltage Range				-2.2		+5.2	V
Differential Input Voltage		$V_{DUT\_}$ - $V_{CHV\_}$, $V_{DUT\_}$ - $V_{CLV\_}$		-7.4		+7.4	V
Hysteresis		$V_{CHV\_}$ = $V_{CLV\_}$ = 1.5V			8		mV
Input Offset Voltage		$V_{DUT\_}$ = 1.5V	A grade			±10	mV
			B grade			±100	
Input Offset Temperature Coefficient					25		µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = 0 and 3V		60			dB
Linearity Error (Note 10)		$V_{DUT\_}$ = 1.5V				±5	mV
		$V_{DUT\_}$ = -2.2V, +5.2V				±10	
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = 1.5V, supplies independently varied over full range				5	mV/V
AC CHARACTERISTICS (Note 11)							
Equivalent Input Bandwidth		Terminated (Note 12)			500		MHz
		High impedance (Note 13)			300		
Propagation Delay					3.9		ns
Prop-Delay Temperature Coefficient					4		ps/°C
Prop-Delay Match, t_{LH} to t_{HL}					120		ps
Prop-Delay Skew, Comparators Within Package		Same edges (LH and HL)			200		ps
Prop-Delay Dispersions vs. Common-Mode Voltage (Note 14)		0 to 4.9V			20		ps
		-1.9V to +4.9V			30		
Prop-Delay Dispersions vs. Overdrive		$V_{CHV\_}$ = $V_{CLV\_}$ = 0.1V to 0.9V, $V_{DUT\_}$ = $1V_{P-P}$, t_R = t_F = 500ps, 10% to 90% relative to timing at 50% point			220		ps
Prop-Delay Dispersions vs. Pulse Width		2ns to 23ns pulse width, relative to 12.5ns pulse width			±60		ps
Prop-Delay Dispersions vs. Slew Rate		0.5V/ns to 2V/ns			50		ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC OUTPUTS							
Reference Voltages COMPHI and COMPLO		(Note 15)		0		+3.6	V
Output High Voltage Offset		I_{OUT} = 0mA, relative to COMPHI at V_{COMPHI} = 1V				±50	mV
Output Low Voltage Offset		I_{OUT} = 0mA, relative to COMPLO at V_{COMPLO} = 0V				±50	mV
Output Resistance		$I_{CHV\_}$ = $I_{CLV\_}$ = ±10mA		40	50	60	Ω
Current Limit					25		mA
Rise/Fall Time		20% to 80%, $V_{CHV\_}$ = $1V_{P-P}$, load = T-line, 50Ω, > 1ns			0.7		ns
PASSIVE LOAD							
DC CHARACTERISTICS ($R_{DUT\_}$ ≥ 10MΩ)							
LDV_ Voltage Range				-2.2		+5.2	V
Gain				0.99		1.01	V/V
Gain Temperature Coefficient					0.02		%/°C
Offset						±100	mV
Offset Temperature Coefficient					0.02		mV/°C
Power-Supply Rejection Ratio	PSRR				10		mV/V
Output Resistance Tolerance—High Value		$I_{DUT\_}$ = ±0.2mA, $V_{LDV\_}$ = 1.5V	A grade	7.125	7.5	7.875	kΩ
			B grade	4.200	6.0	7.875	
Output Resistance Tolerance—Low Value		$I_{DUT\_}$ = ±0.1mA, $V_{LDV\_}$ = 1.5V	A grade	1.90	2.0	2.10	kΩ
			B grade	1.05	1.5	2.10	
Switch Resistance Variation		Relative to 1.5V	0 to 3V		±10		%
			Full range		±30		
Maximum Output Current (Note 16)		$V_{LDV\_}$ = -2V, $V_{DUT\_}$ = +5V			±4		mA
		$V_{LDV\_}$ = +5V, $V_{DUT\_}$ = -2V			±4		
Linearity Error, Full Range		Measured at -2.2V, +1.5V, and +5.2V (Note 16)				±25	mV
AC CHARACTERISTICS							
Settling Time, LDV_ to Output		$V_{LDV\_}$ = -2V to +5V step, $R_{DUT\_}$ = 100kΩ (Note 17)			0.5		µs
Output Transient Response		$V_{LDV\_}$ = +1.5V, $V_{DUT\_}$ = -2V to +5V square wave at 1MHz, $R_{DUT\_}$ = 50Ω			20		ns

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMU SWITCHES (FORCE_, SENSE_, PMU_)						
Voltage Range			-2.2		+5.2	V
Force Switch Resistance		$V_{FORCE\_}$ = 1.5V, $I_{PMU\_}$ = ±10mA			40	Ω
Force Switch Compliance		$V_{PMU\_}$ = 6.2V, $V_{FORCE\_}$ set to make $I_{FORCE\_}$ = 30mA	25			mA
		$V_{PMU\_}$ = -3.2V, $V_{FORCE\_}$ set to make $I_{FORCE\_}$ = -30mA	25			
Force Switch Resistance Variation (Note 18)		0 to 3V		±10		%
		Full range		±30		
Sense Switch Resistance			700	1000	1300	Ω
Sense Switch Resistance Variation		Relative to 1.3V, full range		±30		%
PMU_ Capacitance		Force-and-sense switches open		5		pF
FORCE_ Capacitance				5		pF
SENSE_ Capacitance				0.2		pF
FORCE_ External Capacitance		Allowable external capacitance		2		nF
SENSE_ External Capacitance		Allowable external capacitance		1		nF
FORCE_ and SENSE_ Switching Speed		Connect or disconnect		10		µs
PMU_ Leakage		FORCE EN_ = SENSE EN_ = 0, $V_{FORCE\_}$ = $V_{SENSE\_}$ = -2.2V to +5.2V		±0.5	±5	nA
TOTAL FUNCTION						
DUT_						
Leakage, High-Impedance Mode		Load switches open, $V_{DUT\_}$ = +5.2V, $V_{CLV\_}$ = $V_{CHV\_}$ = -2.2V, $V_{DUT\_}$ = -2.2V, $V_{CLV\_}$ = $V_{CHV\_}$ = +5.2V, full range			2	µA
Leakage, Low-Leakage Mode		Full range		±1	±20	nA
Low-Leakage Recovery Time		(Note 19)		10		µs
Combined Capacitance		Term mode		2		pF
		High-impedance mode		5		
Load Resistance		(Note 20)		1		GΩ
Load Capacitance		(Note 20)		12		nF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE INPUTS (DHV_, DTV_, DLV_, DATA_, RCV_, CHV_, CLV_, LDV_, COMPHI, COMPLO)						
Input Bias Current					±100	µA
Input Bias Current Temperature Coefficient				±200		nA/°C
Settling to Output		0.1% of full-scale step		10		µs
DIGITAL INPUTS (DATA_, RCV_, $\overline{LD}$, DIN, SCLK, $\overline{CS}$)						
Input High Voltage		(Note 21)	V_L / 2 + 0.2		+3.6	V
Input Low Voltage		(Note 21)	-0.3		V_L / 2 - 0.2	V
Input Bias Current					100	µA
SERIAL DATA OUTPUT (DOUT)						
Output High Voltage		I_{OH} = -1mA	V_L - 0.4		V_L	V
Output Low Voltage		I_{OL} = 1mA	0		+0.4	V
Output Rise and Fall Time		C_L = 10pF		1.1		ns
SCLK to DOUT Delay		C_L = 10pF	t_{DH}		t_{SCLK} - t_{DS} - 2ns	ns
SERIAL-INTERFACE TIMING (Note 22)						
SCLK Frequency					50	MHz
SCLK Pulse-Width High	t_{CH}		10			ns
SCLK Pulse-Width Low	t_{CL}		10			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}		0			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		15			ns
DIN to SCLK High Setup	t_{DS}		3.5			ns
DIN to SCLK High Hold	t_{DH}		1			ns
$\overline{CS}$ High to $\overline{LOAD}$ Low Setup	t_{CLL}		6			ns
$\overline{LD}$ Low Hold Time	t_{LDW}		5			ns
$\overline{LD}$ High to Any Activity			0			ns
V_L Rising to $\overline{CS}$ Low		Power-on delay		2		µs
TEMP SENSOR						
Nominal Voltage		T_J = +27°C		3.00		V
Temperature Coefficient				+10		mV/°C
Output Resistance				500		Ω

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

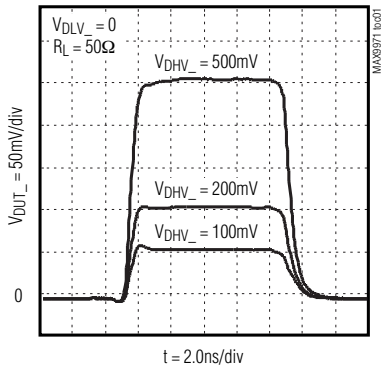
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	(Note 23)	7.6	8	8.4	V
Negative Supply Voltage	V_{SS}	(Note 23)	-5.25	-5	-4.75	V
Logic Supply Voltage	V_L		2.3		3.6	V
Positive Supply Current	I_{DD}	f_{OUT} = 0MHz		97	120	mA
Negative Supply Current	I_{SS}	f_{OUT} = 0MHz		99	120	mA
Logic Supply Current	I_L			0.15	0.30	mA
Static Power Dissipation		f_{OUT} = 0MHz		1.3	1.5	W
Operating Power Dissipation		f_{OUT} = 100Mbps (Note 24)		1.4		W

Note 1: All minimum and maximum specifications are 100% production tested except driver dynamic output current, which is guaranteed by design. All specifications are with DUT_ and PMU_ electrically isolated, unless otherwise noted.
Note 2: Nominal target value is 49.5Ω. Contact factory for alternate trim selections within the 45Ω to 55Ω range.
Note 3: Measured at 1.5V, relative to a straight line through 0 and 3V.
Note 4: Measured at end points, relative to a straight line through 0 and 3V.
Note 5: DUT_ is terminated with 50Ω to ground, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, unless otherwise specified. DATA_ and RCV_ logic levels are V_{HIGH} = 2V, V_{LOW} = 1V.
Note 6: Undershoot is any reflection of the signal back towards its starting voltage after it has reached 90% of its swing. Preshoot is any aberration in the signal before it reaches 10% of its swing.
Note 7: At the minimum voltage swing, undershoot is less than 20%. DHV_ and DLV_ references are adjusted to result in the specified swing.
Note 8: At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.
Note 9: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.
Note 10: Relative to a straight line through 0 and 3V.
Note 11: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to 1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V, t_R = t_F = 500ps, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = +0.5V. Comparator outputs are terminated with 50Ω to GND. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to midpoint of nominal comparator output swing.
Note 12: Terminated is defined as driver in drive mode and set to zero volts.
Note 13: High impedance is defined as driver in high-impedance mode.
Note 14: $V_{DUT\_}$ = 200mV_{P-P}. Propagation delay is compared to a reference time at 1.5V.
Note 15: The comparator meets all its timing specifications with the specified output conditions when the output current is less than 15mA, V_{COMPHI} > V_{COMPLO}, and V_{COMPHI} - V_{COMPLO} ≤ 1V. Higher voltage swings are valid but AC performance may degrade.
Note 16: LOAD EN LOW = LOAD EN HIGH = 1.
Note 17: Waveform settles to within 5% of final value into load 100kΩ.
Note 18: $I_{PMU\_}$ = ±2mA at $V_{FORCE\_}$ = -2.2V, +1.5V, and +5.2V. Percent variation relative to value calculated at $V_{FORCE\_}$ = +1.5V.
Note 19: Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_.
Note 20: Load at end of 2ns transmission line; for stability only, AC performance may be degraded.
Note 21: The driver meets all of its timing specifications over the specified digital input voltage range.
Note 22: Timing characteristics with V_{LOGIC} = 3V.
Note 23: Specifications are simulated and characterized over the full power-supply range. Production tests are performed with power supplies at typical values.
Note 24: All channels driven at 3V_{P-P}, load = 2ns, 50Ω transmission line terminated with 3pF.

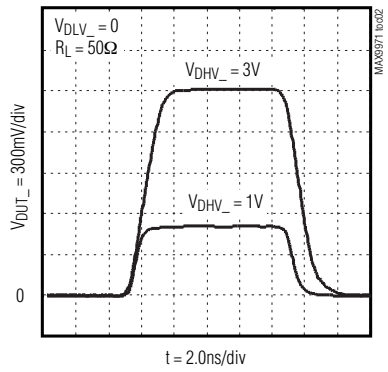
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

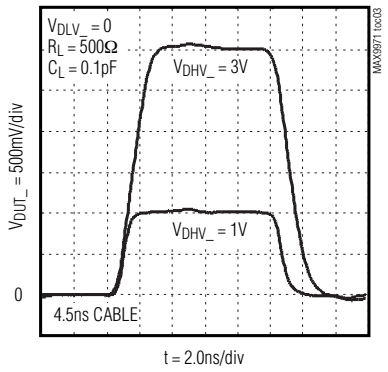
DRIVER SMALL-SIGNAL RESPONSE



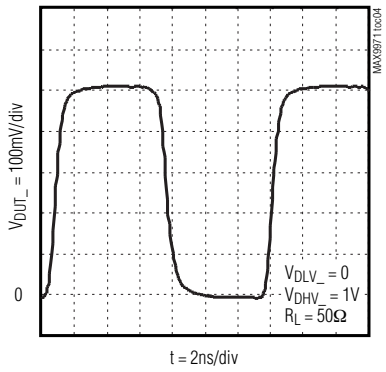
DRIVER LARGE-SIGNAL RESPONSE



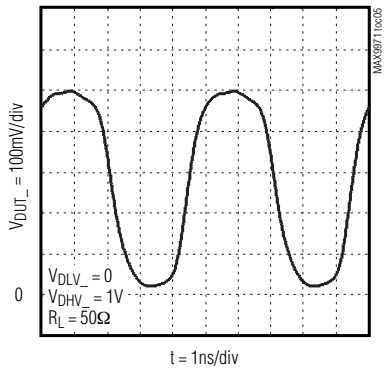
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



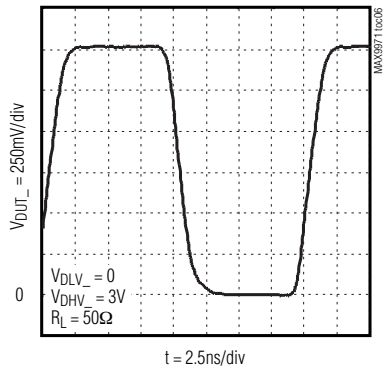
DRIVER 1VP-P, 150Mbps SIGNAL RESPONSE



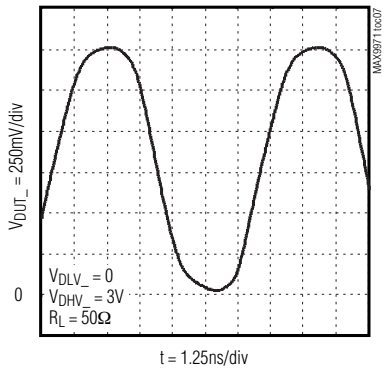
DRIVER 1VP-P, 400Mbps SIGNAL RESPONSE



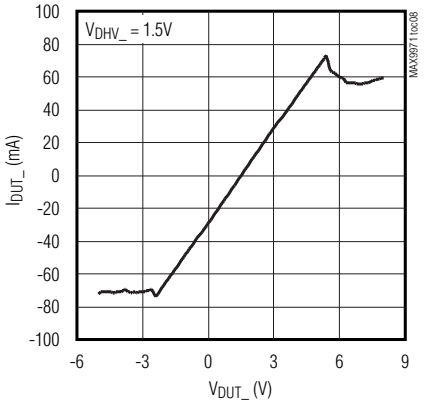
DRIVER 3VP-P, 100Mbps SIGNAL RESPONSE



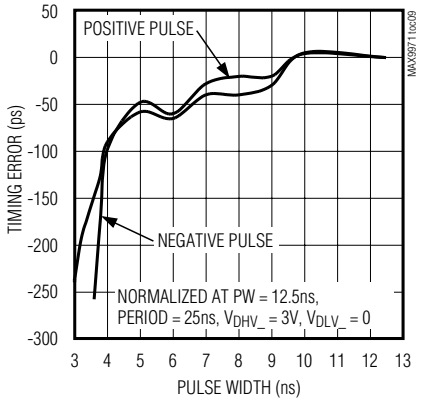
DRIVER 3VP-P, 250Mbps SIGNAL RESPONSE



DRIVER DC CURRENT-LIMIT AND OVERVOLTAGE RESPONSE



DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH

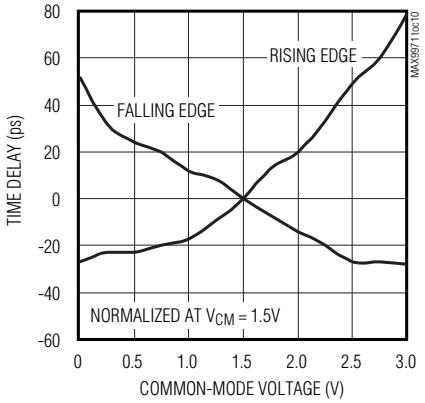


Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

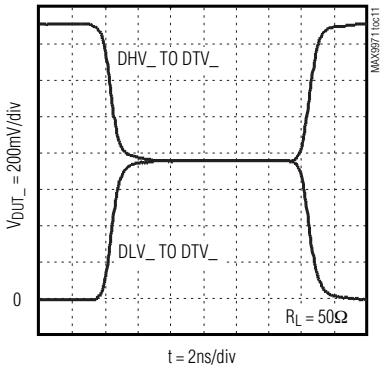
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

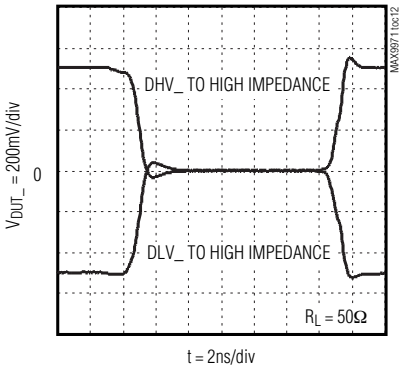
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



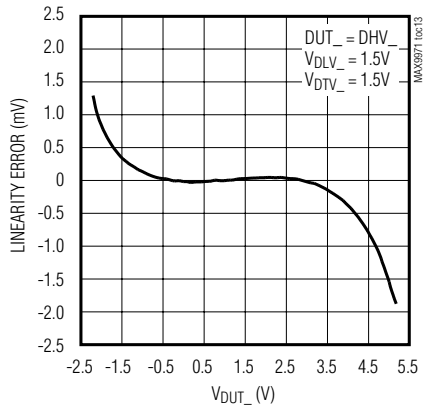
DRIVE-TO-TERM TRANSITION



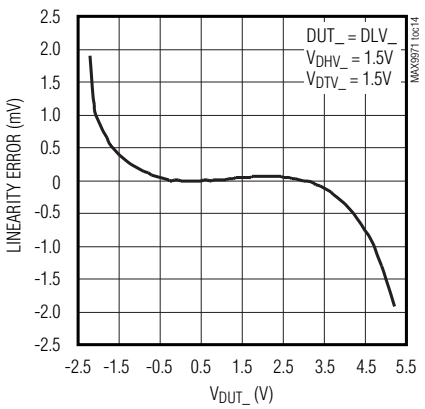
DRIVE-TO-HIGH-IMPEDANCE TRANSITION



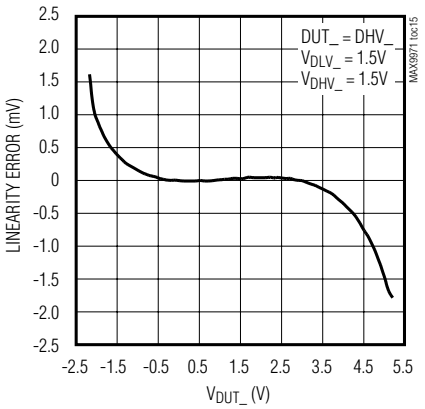
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



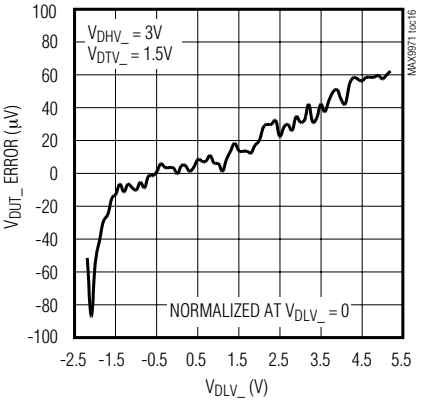
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



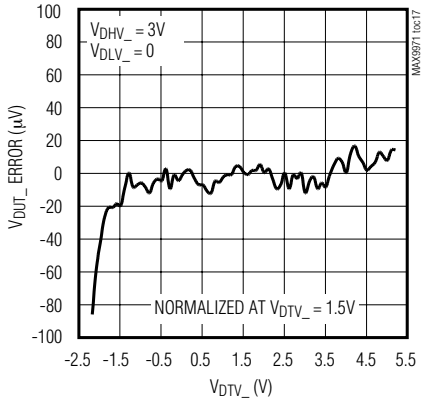
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



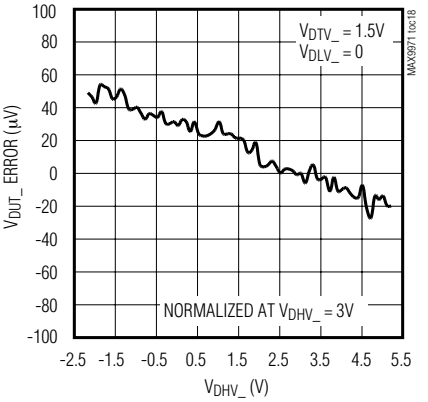
CROSSTALK, DUT_ DRIVEN BY DHV_ WITH DLV_ VARIED



CROSSTALK, DUT_ DRIVEN BY DHV_ WITH DTV_ VARIED



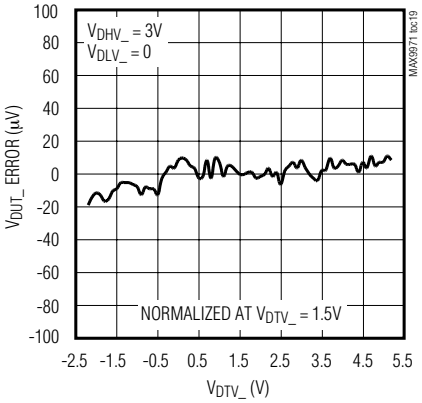
CROSSTALK, DUT_ DRIVEN BY DLV_ WITH DHV_ VARIED



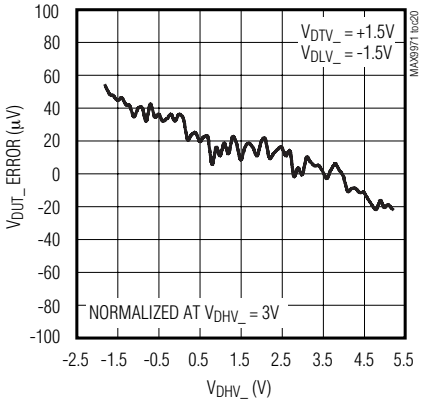
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

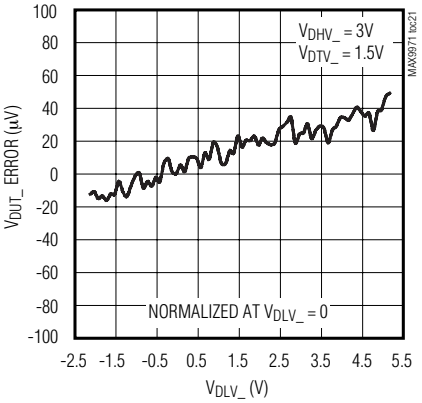
CROSSTALK, DUT_ DRIVEN BY DLV_ WITH DTV_ VARIED



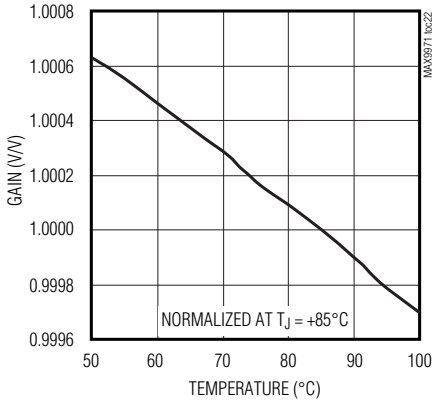
CROSSTALK, DUT_ DRIVEN BY DTV_ WITH DHV_ VARIED



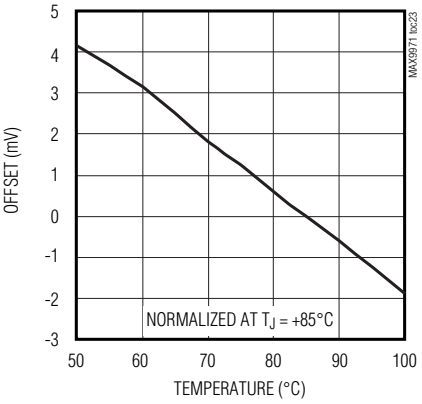
CROSSTALK, DUT_ DRIVEN BY DTV_ WITH DLV_ VARIED



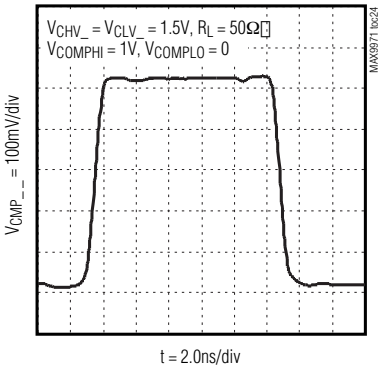
DRIVER GAIN vs. TEMPERATURE



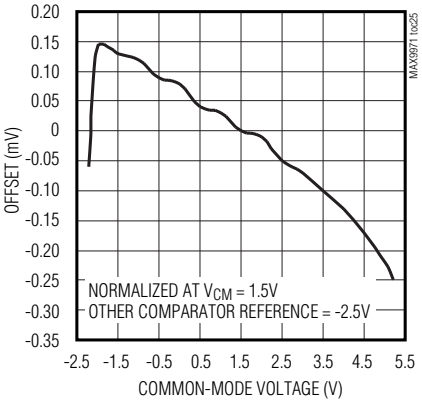
DRIVER OFFSET vs. TEMPERATURE



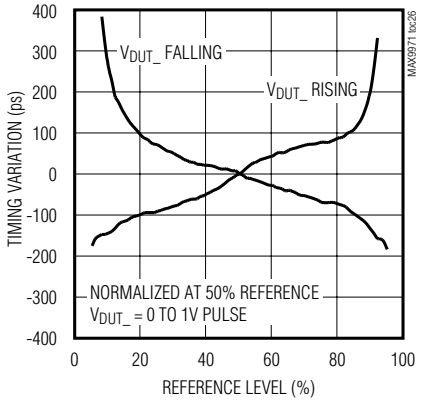
COMPARATOR RESPONSE TO 0 TO 3V SIGNAL



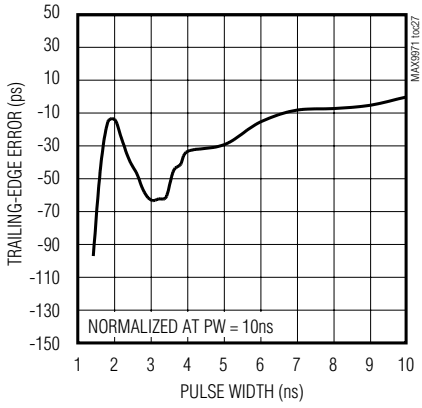
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



COMPARATOR WAVEFORM TRACKING



COMPARATOR TIMING VARIATION vs. PULSE WIDTH

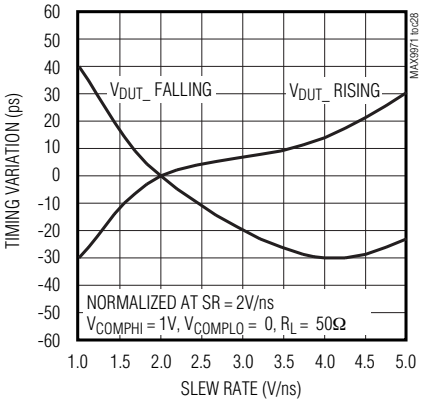


Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

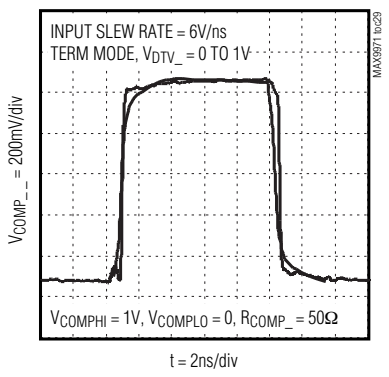
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

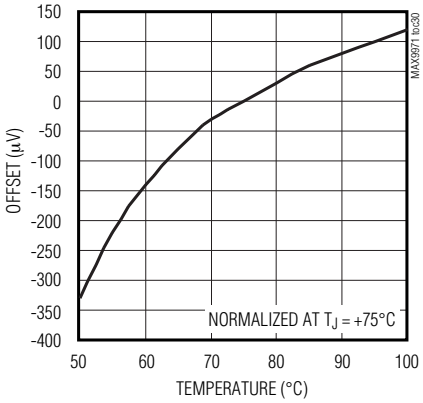
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE



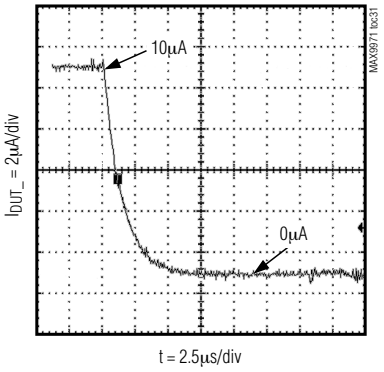
COMPARATOR RESPONSE vs. HIGH SLEW-RATE OVERDRIVE



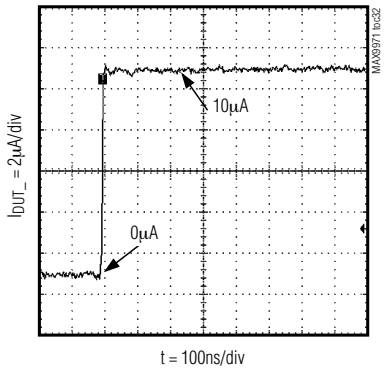
COMPARATOR OFFSET vs. TEMPERATURE



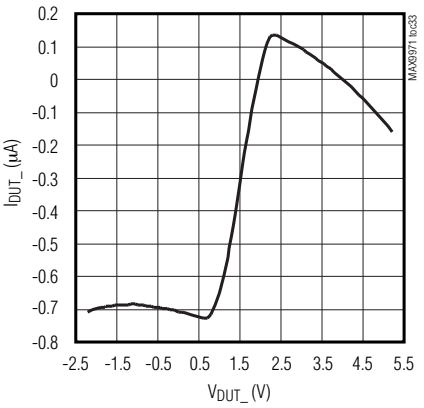
DRIVE 1V TO LOW-LEAKAGE TRANSITION



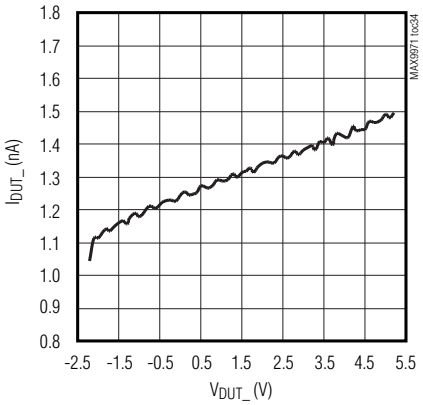
LOW LEAKAGE TO DRIVE 1V TRANSITION



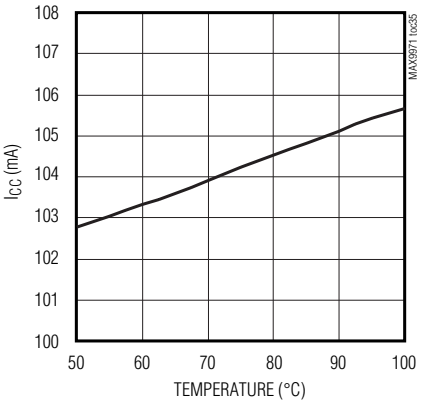
HIGH-IMPEDANCE LEAKAGE AT DUT_ vs. DUT_ VOLTAGE



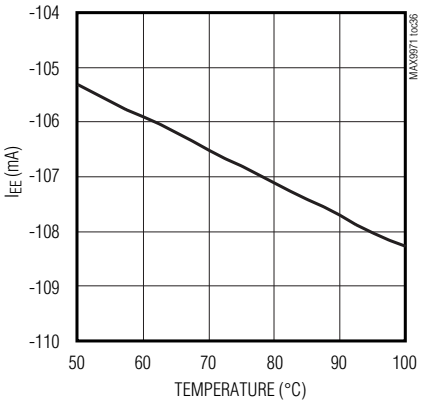
LOW-LEAKAGE CURRENT vs. DUT_VOLTAGE



ICC SUPPLY CURRENT vs.TEMPERATURE



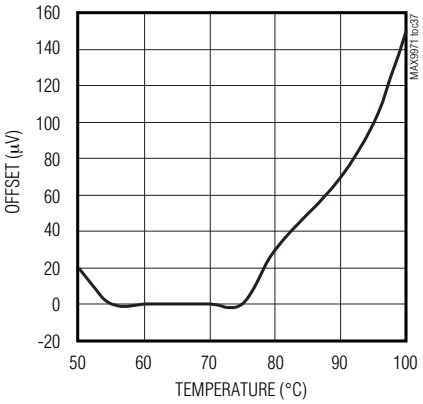
IEE SUPPLY CURRENT vs.TEMPERATURE



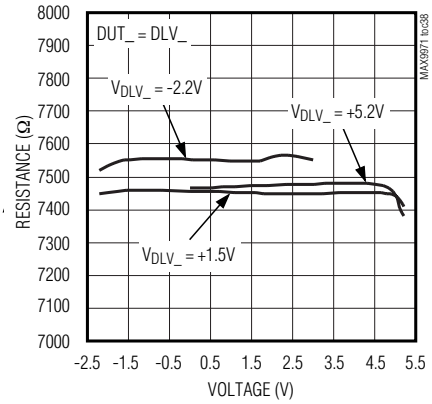
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

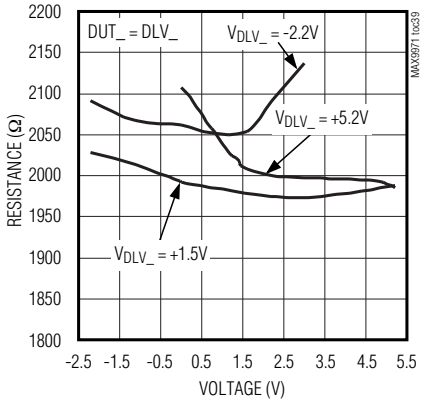
PASSIVE LOAD OFFSET vs. TEMPERATURE



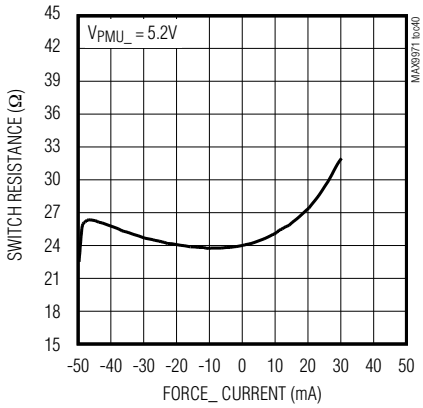
PASSIVE LOAD HIGH RESISTOR vs. VOLTAGE



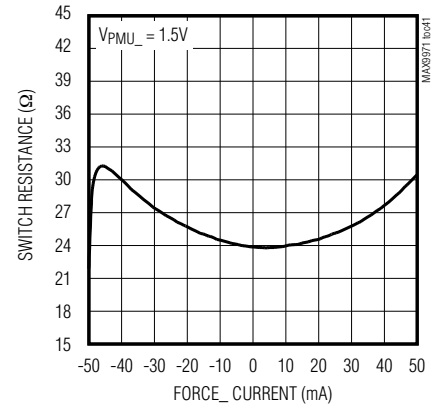
PASSIVE LOAD LOW RESISTOR vs. VOLTAGE



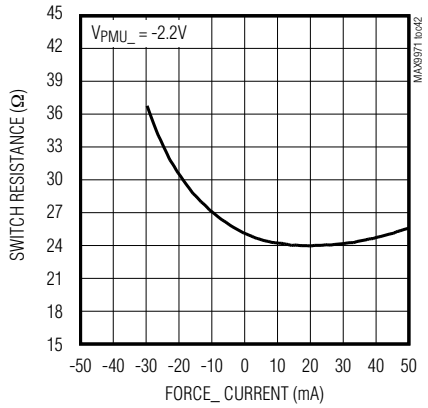
PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

Pin Description

PIN		NAME	FUNCTION
MAX9972	MAX9971		
1	60	DATA1	Channel 1 Multiplexer Control Input. Selects driver 1 input from DHV1 or DLV1 in drive mode. See Table 1 and Figure 2.
2	59	RCV1	Channel 1 Multiplexer Control Input. Sets channel 1 mode to drive or receive. See Table 1 and Figure 2.
3, 8, 13, 18, 51	10, 43, 48, 53, 58	GND	Analog Ground
4	57	CMPH1	Channel 1 High-Side Comparator Output
5	56	CMPL1	Channel 1 Low-Side Comparator Output
6	55	DATA2	Channel 2 Multiplexer Control Input. Selects driver 2 input from DHV2 or DLV2 in drive mode. See Table 1 and Figure 2.
7	54	RCV2	Channel 2 Multiplexer Control Input. Sets channel 2 mode to drive or receive. See Table 1 and Figure 2.
9	52	CMPH2	Channel 2 High-Side Comparator Output
10	51	CMPL2	Channel 2 Low-Side Comparator Output
11	50	CMPL3	Channel 3 Low-Side Comparator Output
12	49	CMPH3	Channel 3 High-Side Comparator Output
14	47	RCV3	Channel 3 Multiplexer Control Input. Sets channel 3 mode to drive or receive. See Table 1 and Figure 2.
15	46	DATA3	Channel 3 Multiplexer Control Input. Selects driver 3 input from DHV3 or DLV3 in drive mode. See Table 1 and Figure 2.
16	45	CMPL4	Channel 4 Low-Side Comparator Output
17	44	CMPH4	Channel 4 High-Side Comparator Output
19	42	RCV4	Channel 4 Multiplexer Control Input. Sets channel 4 mode to drive or receive. See Table 1 and Figure 2.
20	41	DATA4	Channel 4 Multiplexer Control Input. Selects driver 4 input from DHV4 or DLV4 in drive mode. See Table 1 and Figure 2.
21	40	DHV4	Channel 4 Driver High Voltage Input
22	39	DLV4	Channel 4 Driver Low Voltage Input
23	38	DTV4	Channel 4 Driver Termination Voltage Input
24	37	CHV4	Channel 4 Threshold Voltage Input for High-Side Comparator
25	36	CLV4	Channel 4 Threshold Voltage Input for Low-Side Comparator
26	35	DHV3	Channel 3 Driver High Voltage Input
27	34	DLV3	Channel 3 Driver Low Voltage Input
28	33	DTV3	Channel 3 Driver Termination Voltage Input
29	32	CHV3	Channel 3 Threshold Voltage Input for High-Side Comparator
30	31	CLV3	Channel 3 Threshold Voltage Input for Low-Side Comparator
31	30	DGND	Digital Ground Connection
32	29	DOUT	Serial-Interface Data Output
33	28	$\overline{LD}$	Load Input. Latches data from the serial input register to the control register on rising edge. Transparent when low.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9972	MAX9971		
34	27	DIN	Serial-Interface Data Input
35	26	SCLK	Serial Clock
36	25	$\overline{CS}$	Chip Select
37	24	SENSE4	Channel 4 PMU Sense Connection
38	23	FORCE4	Channel 4 PMU Force Connection
39	22	SENSE3	Channel 3 PMU Sense Connection
40	21	FORCE3	Channel 3 PMU Force Connection
41	20	TEMP	Temperature Sensor Output
42, 47, 52, 56, 60	1, 5, 9, 14, 19	V_{DD}	Positive Power-Supply Input
43	18	DUT4	Channel 4 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 4.
44	17	PMU4	Channel 4 Parametric Measurement Connection. PMU switch I/O node for channel 4.
45, 50, 53, 57	4, 8, 11, 16	V_{SS}	Negative Power-Supply Input
46	15	V_L	Logic Power-Supply Input
48	13	DUT3	Channel 3 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 3.
49	12	PMU3	Channel 3 Parametric Measurement Connection. PMU switch I/O node for channel 3.
54	7	PMU2	Channel 2 Parametric Measurement Connection. PMU switch I/O node for channel 2.
55	6	DUT2	Channel 2 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 2.
58	3	PMU1	Channel 1 Parametric Measurement Connection. PMU switch I/O node for channel 1.
59	2	DUT1	Channel 1 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 1.
61	80	FORCE2	Channel 2 PMU Force Connection
62	79	SENSE2	Channel 2 PMU Sense Connection
63	78	FORCE1	Channel 1 PMU Force Connection
64	77	SENSE1	Channel 1 PMU Sense Connection
65	76	COMPLO	Comparator Output-Low Voltage Reference Input
66	75	COMPHI	Comparator Output-High Voltage Reference Input
67	74	LDV4	Channel 4 Load Voltage Input
68	73	LDV3	Channel 3 Load Voltage Input
69	72	LDV2	Channel 2 Load Voltage Input
70	71	LDV1	Channel 1 Load Voltage Input
71	70	CLV2	Channel 2 Threshold Voltage Input for Low-Side Comparator
72	69	CHV2	Channel 2 Threshold Voltage Input for High-Side Comparator
73	68	DTV2	Channel 2 Driver Termination Voltage Input
74	67	DLV2	Channel 2 Driver Low Voltage Input
75	66	DHV2	Channel 2 Driver High Voltage Input
76	65	CLV1	Channel 1 Threshold Voltage Input for Low-Side Comparator
77	64	CHV1	Channel 1 Threshold Voltage Input for High-Side Comparator
78	63	DTV1	Channel 1 Driver Termination Voltage Input
79	62	DLV1	Channel 1 Driver Low Voltage Input
80	61	DHV1	Channel 1 Driver High Voltage Input
—	—	EP	Exposed Pad. Leave unconnected or connect to V_{SS}.

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

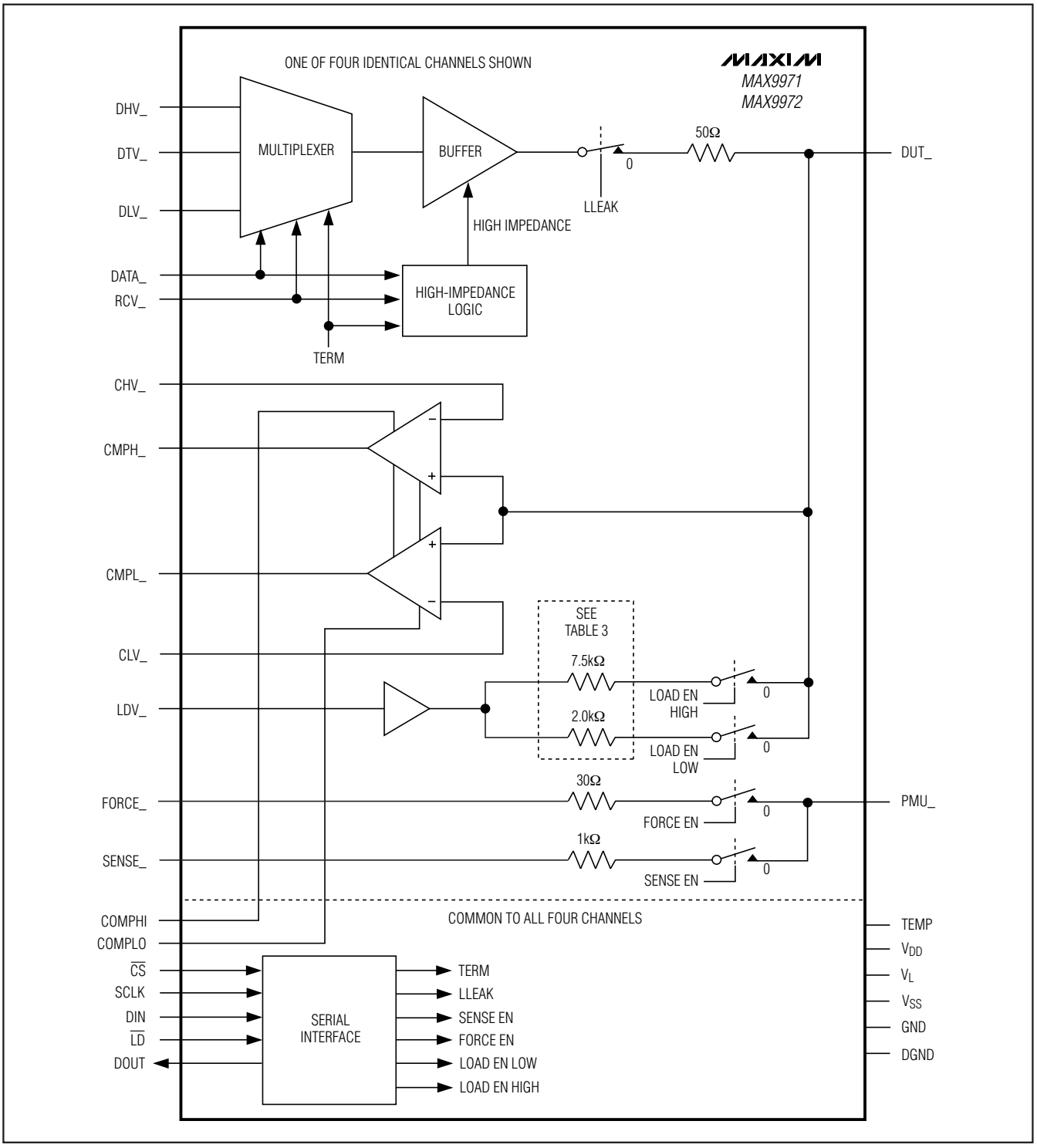


Figure 1. Block Diagram

Detailed Description

The MAX9971/MAX9972 are four-channel, pin-electronics ICs for automated test equipment that include, for each channel, a three-level pin driver, a window comparator, a passive load, and a Kelvin instrument connection (Figure 1). All functions feature a -2.2V to +5.2V operating range and the drivers include both high-impedance and active-termination (3rd-level drive) modes. The comparators feature programmable output voltages, allowing optimization for different CMOS interface standards. The loads have selectable output resistance for optimizing DUT current loading. The Kelvin paths allow accurate connection of an instrument with ±25mA source/sink capability. Additionally, the MAX9971/MAX9972 offer a low-leakage mode that reduces DUT_ leakage current to less than 20nA.

The MAX9971/MAX9972 are available in two grades. The A-grade devices provide tighter tolerances for driver gains and offsets, comparator offsets, and load resistor values. This allows reference levels to be shared across multiple channels in cost-sensitive systems. The B-grade devices are intended for system designs that incorporate independent reference levels for each channel.

Each of the four channels feature single-ended CMOS-compatible inputs, DATA_ and RCV_, for control of the driver signal path (Figure 2). The MAX9971/MAX9972 modal operation is programmed through a 3-wire, low-voltage CMOS-compatible serial interface.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs; DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_, and mode-control bit TERM (Table 1). DATA_ and RCV_ are single-ended inputs with threshold levels equal to V_L / 2. Each channel's threshold levels are independently generated to minimize crosstalk.

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). High-speed input RCV_ and mode-control bits TERM and LLEAK control these modes. In high-impedance mode, the bias current at DUT_ is less than 2µA over the -2.2V to +5.2V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 20nA, and signal tracking slows.

The nominal driver output resistance is 50Ω. Custom resistance values from 45Ω to 51Ω are possible; consult factory for further information.

Table 1. Driver Channel Control Signals

EXTERNAL CONNECTIONS		INTERNAL CONTROL BITS		DRIVER OUTPUT	DRIVER MODE
RCV_	DATA_	TERM	LLEAK		
0	0	X	0	DUT_ = DLV_	Drive
0	1	X	0	DUT_ = DHV_	Drive
1	X	0	0	High Impedance	Receive
1	X	1	0	DUT_ = DTV_	Receive
X	X	X	1	Low Leak	Low Leakage

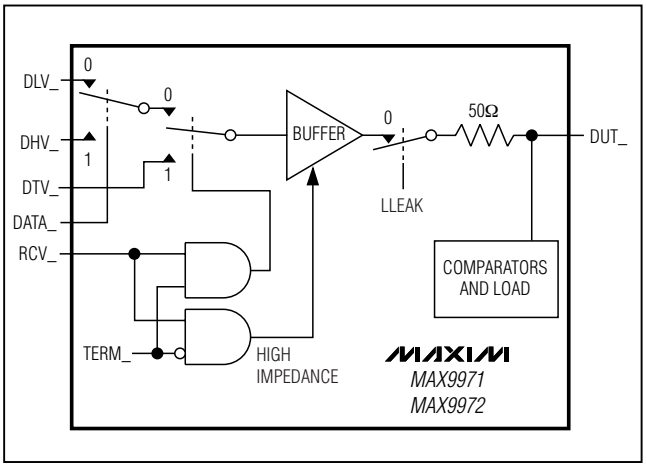


Figure 2. Multiplexer and Driver Channel

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

Comparators

The MAX9971/MAX9972 provide two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (see Figure 1). Comparator outputs are a logical result of the input conditions, as indicated in Table 2.

The comparator output voltages are easily interfaced to a wide variety of logic standards. Use buffered inputs COMPHI and COMPLO to set the high and low output voltages. For correct operation, COMPHI should be greater than or equal to COMPLO. The comparator 50Ω output impedance provides source termination (Figure 3).

Passive Load

The MAX9971/MAX9972 channels each feature a passive load consisting of a buffered input voltage, LDV_, connected to DUT_ through two resistive paths (Figure 1). Each path connects to DUT_ individually by a switch controlled through the serial interface. Programming options include none (load disconnected), either, or both paths connected. The resistor values vary depending on the accuracy grade of the device, as shown in Table 3. The loads facilitate fast open/short testing in conjunction with the comparator, and pullup of open-drain DUT_ outputs.

Parametric Switches

Each of the four MAX9971/MAX9972 channels provides force-and-sense paths for connection of a PMU or other DC resource to the device-under-test (Figure 1). Each force-and-sense switch is independently controlled though the serial interface providing maximum application flexibility. PMU_ and DUT_ are provided on separate pins allowing designs that do not require the parametric switch feature to avoid the added capacitance of PMU_. It also allows PMU_ to connect to DUT_ either directly or with an impedance-matching network.

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port places the MAX9971/MAX9972 into a very-low-leakage state (see the *Electrical Characteristics* table). This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK control is independent for each channel.

When DUT_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Table 2. Comparator Logic

DUT_ > CHV_	DUT_ > CLV_	CMPH_	CMPL_
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

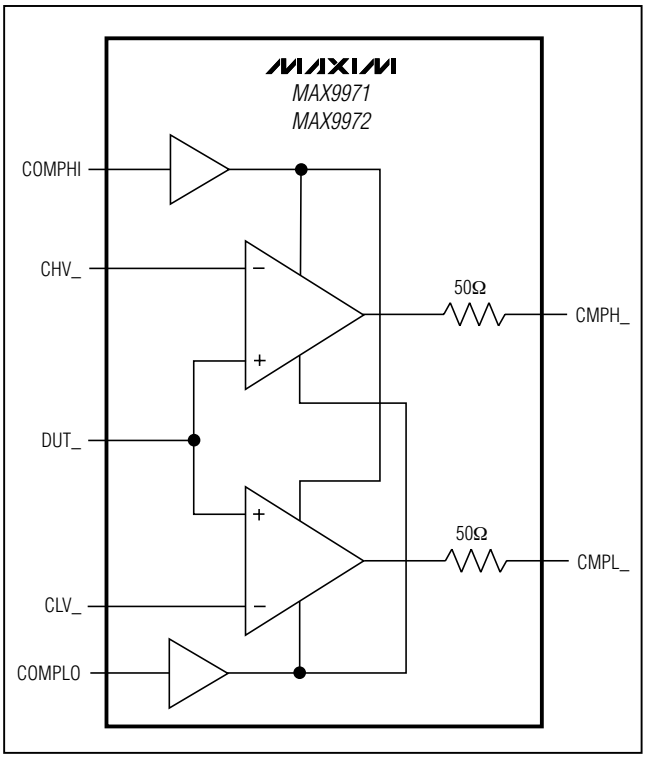


Figure 3. Complementary 50Ω Comparator Outputs

Table 3. Passive Load Resistance Values

ACCURACY GRADE	HIGH RESISTOR (kΩ)	LOW RESISTER (kΩ)
A	7.5	2
B	6	1.5

Temperature Monitor

Each device supplies a single temperature output signal, TEMP, that asserts a nominal 3.43V output voltage at a +70°C (343K) die temperature. The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 500Ω, typical.

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9971/MAX9972 modes (Figure 4). Control data flow into a 12-bit shift register (MSB first) and are latched when $\overline{CS}$ is taken high. Data from the shift register are then loaded to the per-channel control latches as determined by bits D8–D11, and indicated in Figure 4 and Table 4. The latches contain the six mode bits for each channel of the device. The mode bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel. Transfer data asynchronously from the input registers to the channel registers by forcing $\overline{LD}$ low. With $\overline{LD}$ always low, data transfer on the rising edge of $\overline{CS}$.

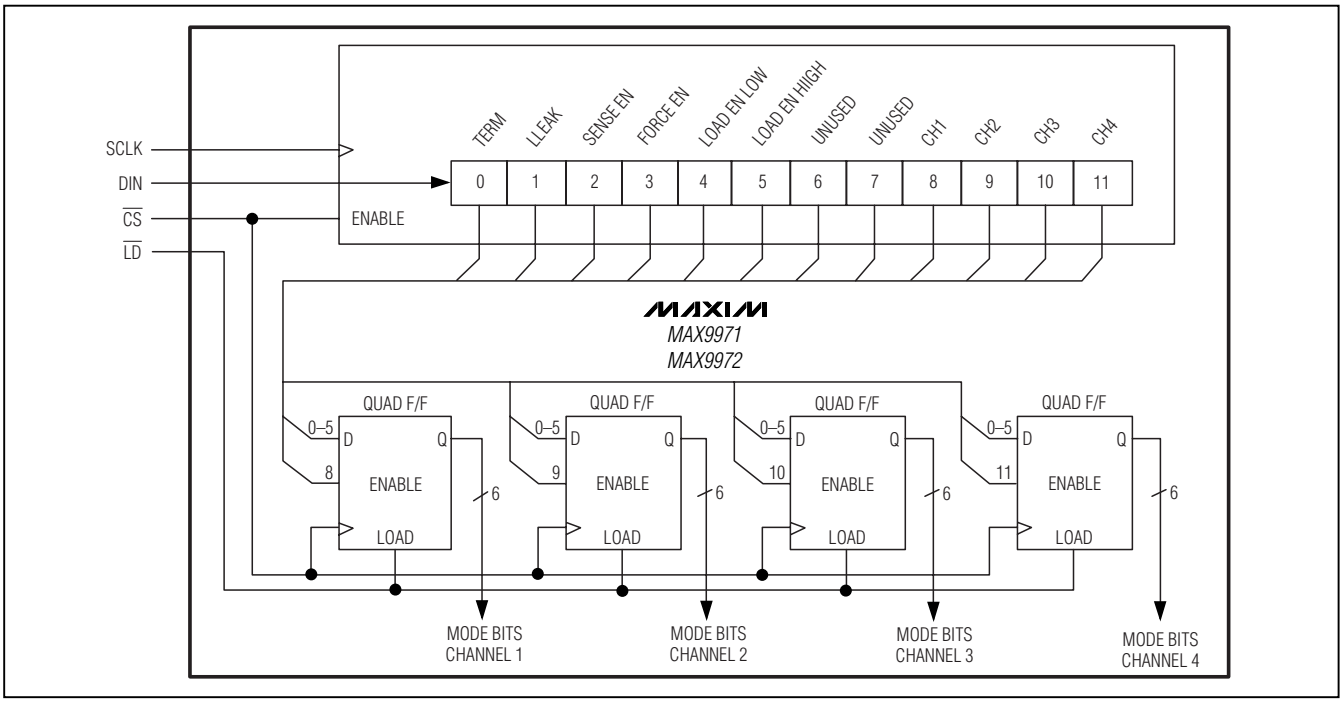


Figure 4. Serial Interface

Table 4. Control Register Bit Functions

BIT	NAME	FUNCTION	BIT STATE		POWER-UP STATE
			0	1	
0	TERM	Term Mode Control	High Impedance	Term Mode	0
1	LLEAK	Assert Low-Leakage Mode	Term Mode	Low Leakage	0
2	SENSE EN	Enable Sense Switch	Disabled	Enabled	0
3	FORCE EN	Enable Force Switch	Disabled	Enabled	0
4	LOAD EN LOW	Enable Low Load Resistor	Disabled	Enabled	0
5	LOAD EN HIGH	Enable High Load Resistor	Disabled	Enabled	0
6	—	Unused	X	X	0
7	—	Unused	X	X	0
8	CH1	Update Channel 1 Control Register	Disabled	Enabled	1
9	CH2	Update Channel 2 Control Register	Disabled	Enabled	1
10	CH3	Update Channel 3 Control Register	Disabled	Enabled	1
11	CH4	Update Channel 4 Control Register	Disabled	Enabled	1

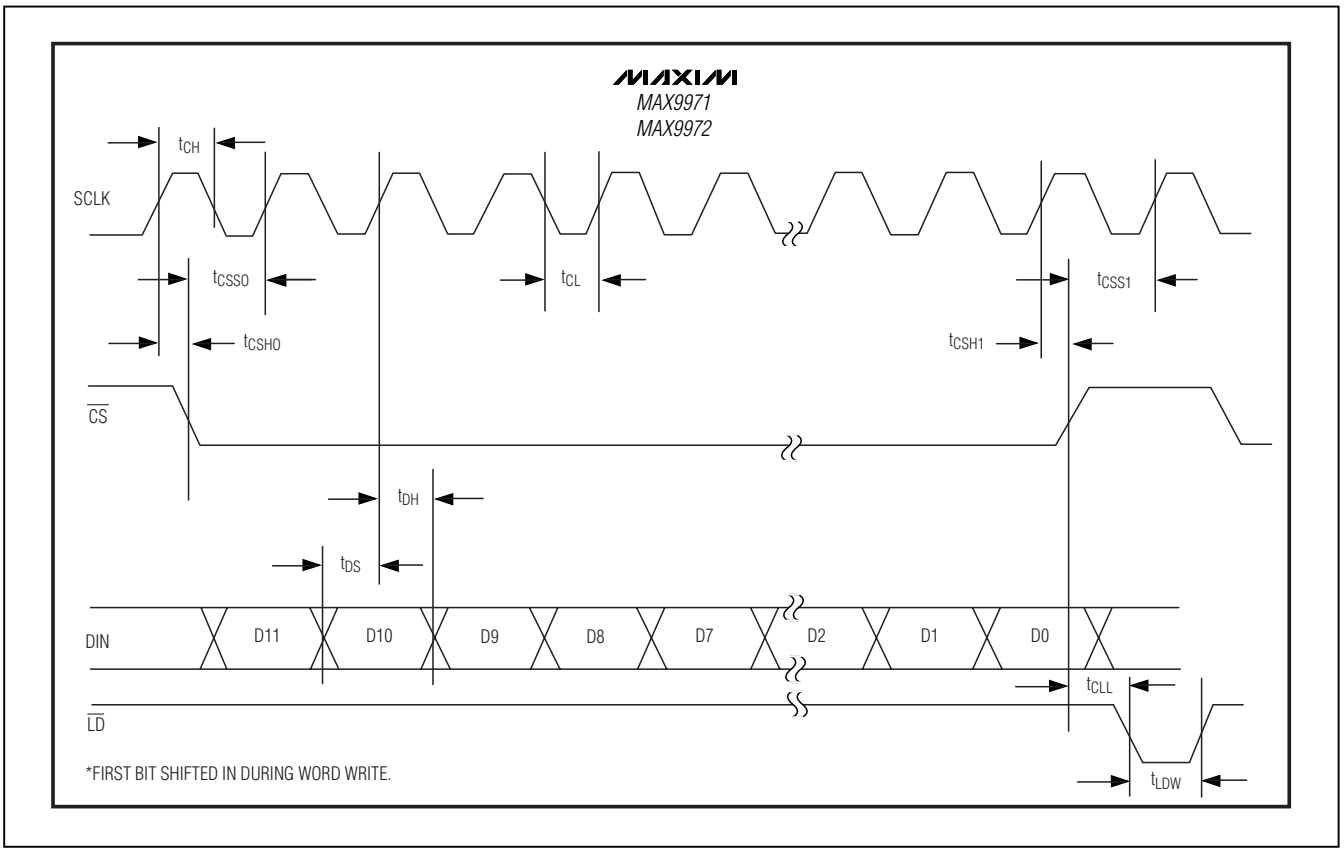


Figure 5. Serial-Interface Timing

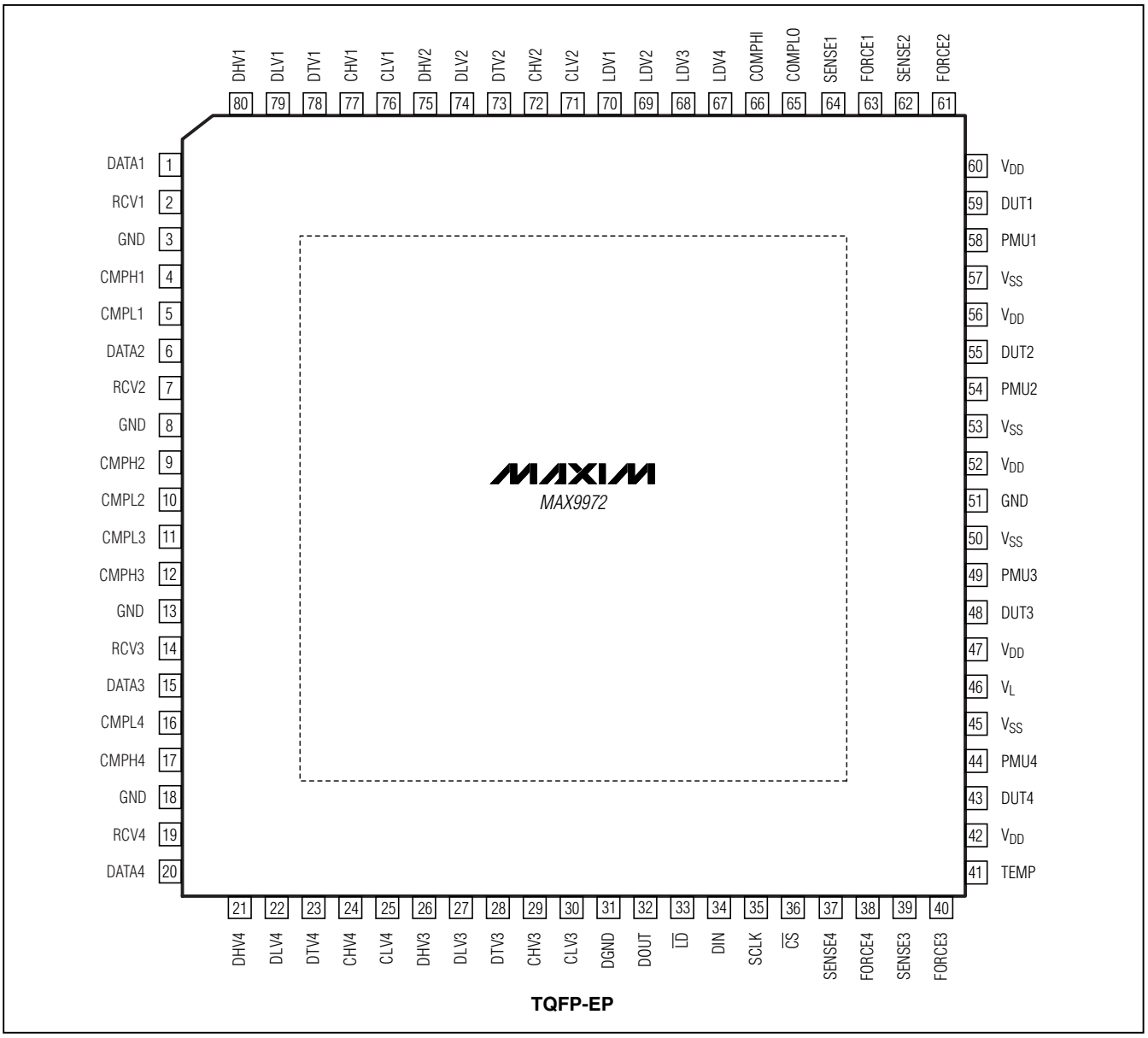
Heat Removal

With adequate airflow, no external heat sinking is needed under most operating conditions. If excess heat must be dissipated through the exposed paddle, solder it to circuit board copper (MAX9972) or use an external heat sink (MAX9971). The exposed paddle must be either left unconnected, isolated, or connected to V_{SS}.

Power Minimization

To minimize power consumption, activate only the needed channels. Each channel placed in low-leakage mode saves approximately 240mW.

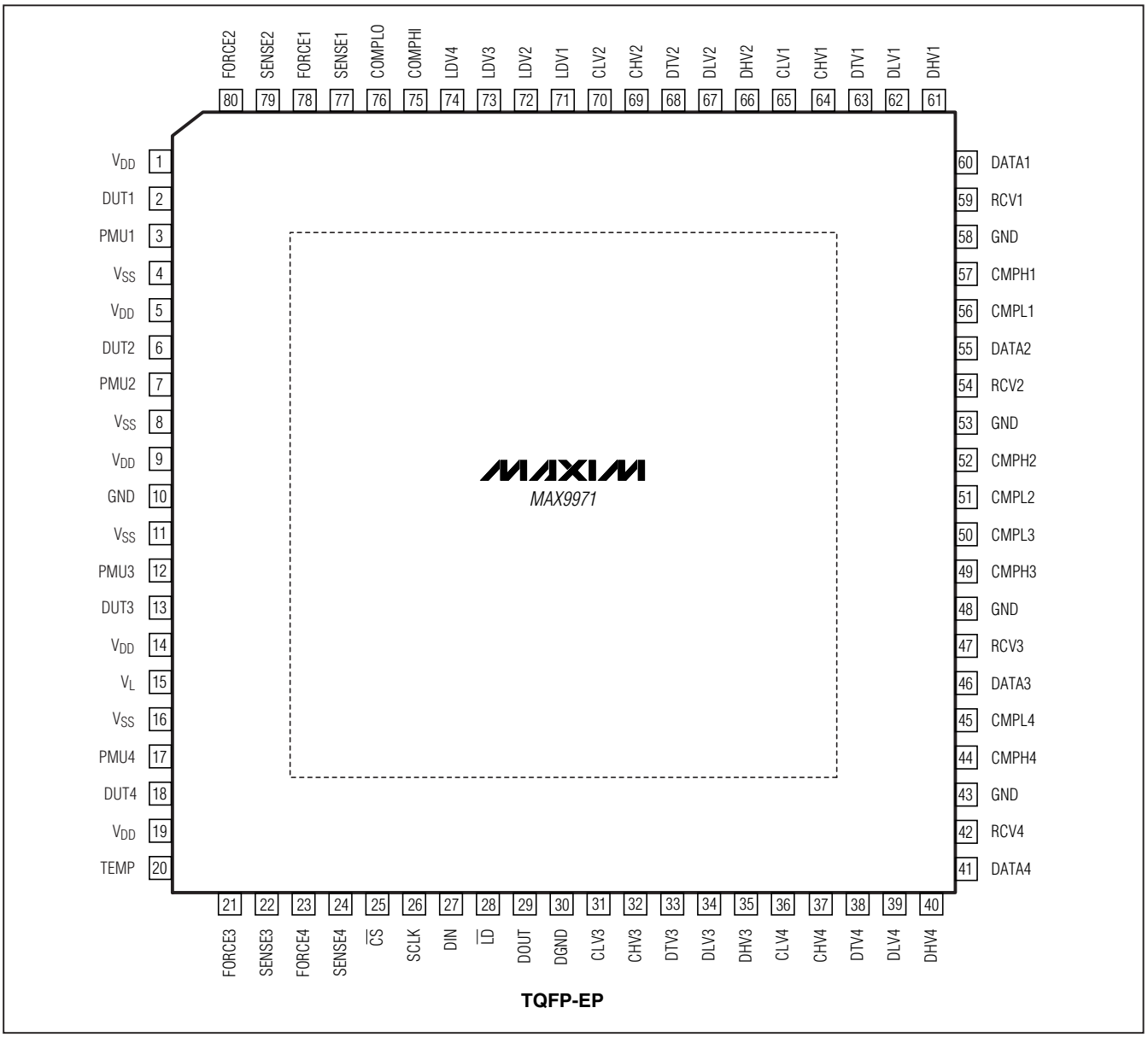
Pin Configurations



TQFP-EP

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

Pin Configurations (continued)



TQFP-EP

Chip Information

TRANSISTOR COUNT: 5728

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

News Release

FOR IMMEDIATE RELEASE

Nextest Showcases a Range of Test Solutions at SEMICON/West 2007

SAN FRANCISCO, California—July 16, 2007—Nextest Systems Corporation (NASDAQ: NEXT), a leading manufacturer of automatic test equipment (ATE) for cost-sensitive semiconductors, announced that it will exhibit a wide range of test solutions at SEMICON/West this year. The conference is being held at the Moscone West Convention Center in San Francisco, California, July 17-19, 2007. The conference provides a venue for semiconductor equipment makers to promote their company, products and services, to chip-making companies from around the world.

Showcased in Nextest's booth #8441, at SEMICON/West this year, are test solutions that demonstrate the Magnum's product family test systems; ranging from 256 pins, up to 7680 pins, and capable of testing a variety of devices, including: NAND, SOC, and logic semiconductors.

MAGNUM Grande™ 7680-pin Test System

To address the industry-wide concern over escalating test costs and capacity requirements, Nextest will demonstrate Magnum's unique architecture that provides customers with the flexibility to add functionality and pin count without system downtime, or software reconfiguration.

At Semicon/West 2005, Magnum displayed 320 devices in parallel. At that same show in 2006, that number soared to 720 parts in parallel. This year, Magnum Grande's 7,680 I/O pin test system will be integrated with a Mirae Model 530 handler—capable of testing 960 NAND flash devices in parallel. To date, this is the highest number of devices being tested in parallel.

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MAGNUM SV™ 1024-pin Test System

Demonstrating Magnum's logic test capability, the Magnum SV is a production test system targeted at FPGA devices. This system is the ideal solution for test requirements of high pin count devices in parallel and provides a flexible pattern architecture for logic and memory test on-the-fly. Also being demonstrated is Nextest's logic Wavetool software that dramatically reduces test program development time.

MAGNUM iCP-EV™ 128-pin Test System

Also on display, the Magnum ICP-EV will be integrated with an Interaction IAOPT-15ONE Illuminator. Focused at the CMOS Image Sensor (CIS) market, Magnum iCP-EV offers CIS manufacturers a low-cost engineering alternative for program development and debug. Due to the system's small physical size, engineering can perform the necessary work in an office environment, prior to moving devices to the Magnum iCP for volume-production testing. This innovative approach allows for a smooth transition to test CIS devices in parallel and is a much more cost-effective method over utilizing expensive, "large-iron" test equipment. CIS devices are being utilized in numerous consumer products such as cell phones, still cameras, web cams, PDA's, and security cameras.

ABOUT NEXTEST

Nextest Systems Corporation is a low-cost leader in the design and manufacture of automatic test equipment (ATE) for Flash memory and System-On-Chip semiconductors. Nextest's products address the growing demand from manufacturers for ATE with increased throughput, functionality and reliability, while reducing time to market and cost of test. Nextest has shipped over 1,800 systems to more than 60 semiconductor companies worldwide. Further information is available at www.nextest.com.

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News Release

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19-0474; Rev 0; 6/06

MAXIM

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

General Description

The MAX9971/MAX9972 four-channel, ultra-low-power, pin-electronics ICs include, for each channel, a three-level pin driver, a window comparator, a passive load, and force-and-sense Kelvin-switched parametric measurement unit (PMU) connections. The driver features a -2.2V to +5.2V voltage range, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The window comparator features 500MHz equivalent input bandwidth and programmable output voltage levels. The passive load provides pullup and pulldown voltages to the device-under-test (DUT).

Two grade versions are available, A grade and B grade. The A-grade version provides tight gain and offset matching for the driver and comparator, allowing reference levels to be shared across multiple channels. It also provides tighter tolerance of the load resistance values. The B-grade version is for system designs that incorporate independent reference levels for each channel.

Low-leakage, high-impedance, and terminate controls are operational configurations that are programmed through a 3-wire, low-voltage, CMOS-compatible serial interface. High-speed PMU switching is realized through dedicated digital control inputs.

These devices are available in an 80-pin, 12mm x 12mm body, 1.0mm pitch TQFP with an exposed 6mm x 6mm die pad on the bottom of the package (MAX9972), and the top of the package (MAX9971), for efficient heat removal. The MAX9971/MAX9972 are specified to operate over the 0°C to +70°C commercial temperature range, and feature a die temperature monitor output.

Applications

NAND Flash Testers

DRAM Probe Testers

Low-Cost Mixed-Signal/System-on-Chip (SOC) Testers

Active Burn-In Systems

Structural Testers

Features

- **Small Footprint—Four Channels in 0.3in²**
- **Low-Power Dissipation: 325mW/Channel Typical**
- **High Speed: 300Mbps at $3V_{P-P}$**
- **-2.2V to +5.2V Operating Range**
- **Active Termination (3rd-Level Drive)**
- **Integrated PMU Switches**
- **Passive Load**
- **Low-Leak Mode: 20nA max**
- **Low Gain and Offset Error**
- **Lead-Free Package Available**

Pin Configurations appear at end of data sheet.

Ordering Information and Selector Guide

PART	ACCURACY GRADE	PIN-PACKAGE	PKG CODE	HEAT EXTRACTION
MAX9971ACCS*	A	80 TQFP-IDP†	—	Top
MAX9971BCCS*	B	80 TQFP-IDP†	—	Top
MAX9972ACCS*	A	80 TQFP-EP††	C80E-4	Bottom
MAX9972BCCS	B	80 TQFP-EP††	C80E-4	Bottom

**Future product—contact factory for availability.*

Note: *All devices are specified over the 0°C to +70°C operating temperature range.*

All versions available in both leaded and lead-free packaging. Specify lead-free by adding the "+" symbol at the end of the part number when ordering.

†*IDP = Inverted die pad.*

††*EP = Exposed paddle.*

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +9.4V
V_{SS} to GND .....-6.25V to +0.3V
V_{DD} to V_{SS} .....+15.7V
V_L to GND .....-0.3V to +5V
V_{DD} to GND .....-0.3V to +9.4V
DHV_, DTV_, DLV_, DATA_, RCV_, LDV_, DUT_ to GND .....V_{SS} to V_{DD}
CHV_, CLV_, CMPH_, CMPL_, COMPHI, COMPLO to GND .....V_{SS} to V_{DD}
FORCE_, SENSE_, PMU_ to GND .....V_{SS} to V_{DD}
$\overline{LD}$, DIN, SCLK, $\overline{CS}$ to GND .....-0.3V to +5V
DUT_, CMPH_, CMPL_ Short-Circuit Duration .....Continuous
DHV_, DLV_, DTV_ to Each Other .....V_{SS} to V_{DD}
CHV_, CLV_ to DUT_ .....V_{SS} to V_{DD}
DOUT to GND .....-0.3V to +5V
TEMP Short-Circuit Duration .....Continuous
Continuous Power Dissipation (T_A = +70°C)
80-Pin TQFP-EP (derate 35.7mW/°C above +70°C) 2857mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER (all specifications apply when DUT_ = DHV_, DUT_ = DTV_, or DUT_ = DLV_)							
DC CHARACTERISTICS							
Voltage Range				-2.2		+5.2	V
Gain		Measured at 0 and 3V	A grade	0.995	1	1.005	V/V
			B grade	0.95		1.05	
Gain Temperature Coefficient					50		ppm/°C
Offset		$V_{DHV\_}$ = 2V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1V	A grade			±7	mV
			B grade			±100	
Offset Temperature Coefficient					±250		µV/°C
Power-Supply Rejection Ratio	PSRR	V_{DD}, V_{SS} independently varied over full range				18	mV/V
Maximum DC Drive Current	$I_{DUT\_}$			±40		±90	mA
DC Output Resistance		$I_{DUT\_}$ = ±10mA (Note 2)		48.5	49.5	50.5	Ω
DC Output Resistance Variation		$I_{DUT\_}$ = -40mA to +40mA				2.5	Ω
DC Crosstalk		DHV to DLV and DTV: $V_{DLV\_}$ = $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -2.2V, +5.2V				5	mV
		DLV to DHV and DTV: $V_{DHV\_}$ = $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -2.2V, +5.2V				5	
		DTV to DHV and DLV: $V_{DHV\_}$ = $V_{DLV\_}$ = +1.5V, $V_{DTV\_}$ = -2.2V, +5.2V				5	
Linearity Error		0 to 3V (Note 3)				±5	mV
		Full range (Note 4)				±15	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (Note 5)						
Dynamic Output Current		(Note 1)	40			mA
Drive-Mode Overshoot, Undershoot, and Preshoot		200mV to 4V_{P-P} swing (Note 6)		5% +10		mV
Term-Mode Spike		$V_{DHV\_}$ = $V_{DTV\_}$ = 1V, $V_{DLV\_}$ = 0		25		mV
		$V_{DLV\_}$ = $V_{DTV\_}$ = 0, $V_{DHV\_}$ = 1V		25		
High-Impedance-Mode Spike		$V_{DLV\_}$ = -1.0V, $V_{DHV\_}$ = 0		25		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		25		
Prop Delay, Data to Output				2		ns
Prop-Delay Temperature Coefficient				10		ps/°C
Prop-Delay Match, t_{LH} vs. t_{HL}				30		ps
Prop-Delay Skew, Drivers Within Package				150		ps
Prop-Delay Change vs. Pulse Width		Relative to 12.5ns pulse; 3V_{P-P}, 40MHz, PW = 4ns to 21ns		20		ps
		Relative to 12.5ns pulse; 1V_{P-P}, 40MHz, PW = 2.5ns to 23.5ns		90		
Prop-Delay Change vs. Common-Mode Voltage		1V_{P-P}, $V_{DLV\_}$ = 0 to 3V, relative to delay at $V_{DLV\_}$ = 1V		80		ps
Prop Delay, Data to High Impedance		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V, both directions		1.8		ns
Prop Delay, Data to Term		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 0, both directions		1.6		ns
Minimum Voltage Swing		(Note 7)		25		mV
Rise/Fall Time		$V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0, 20% to 80%		0.7		ns
		$V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0, 20% to 80%		0.7		
		$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 10% to 90%	1.5	2.0	2.5	
		$V_{DHV\_}$ = 4V, $V_{DLV\_}$ = 0, R_L = 500Ω, 10% to 90%		2.6		
		$V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0, R_L = 500Ω, 10% to 90%		3.4		
Rise/Fall-Time Matching		$V_{DHV\_}$ = 1V to 5V		±5		%
Minimum Pulse Width (Note 8)		200mV, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0		1.8		ns
		1V, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0		2.4		
		3V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0		3.3		

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR (Note 9)							
DC CHARACTERISTICS (driver in high-impedance mode)							
Input Voltage Range				-2.2		+5.2	V
Differential Input Voltage		$V_{DUT\_}$ - $V_{CHV\_}$, $V_{DUT\_}$ - $V_{CLV\_}$		-7.4		+7.4	V
Hysteresis		$V_{CHV\_}$ = $V_{CLV\_}$ = 1.5V			8		mV
Input Offset Voltage		$V_{DUT\_}$ = 1.5V	A grade			±10	mV
			B grade			±100	
Input Offset Temperature Coefficient					25		µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = 0 and 3V		60			dB
Linearity Error (Note 10)		$V_{DUT\_}$ = 1.5V				±5	mV
		$V_{DUT\_}$ = -2.2V, +5.2V				±10	
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = 1.5V, supplies independently varied over full range				5	mV/V
AC CHARACTERISTICS (Note 11)							
Equivalent Input Bandwidth		Terminated (Note 12)			500		MHz
		High impedance (Note 13)			300		
Propagation Delay					3.9		ns
Prop-Delay Temperature Coefficient					4		ps/°C
Prop-Delay Match, t_{LH} to t_{HL}					120		ps
Prop-Delay Skew, Comparators Within Package		Same edges (LH and HL)			200		ps
Prop-Delay Dispersions vs. Common-Mode Voltage (Note 14)		0 to 4.9V			20		ps
		-1.9V to +4.9V			30		
Prop-Delay Dispersions vs. Overdrive		$V_{CHV\_}$ = $V_{CLV\_}$ = 0.1V to 0.9V, $V_{DUT\_}$ = $1V_{P-P}$, t_R = t_F = 500ps, 10% to 90% relative to timing at 50% point			220		ps
Prop-Delay Dispersions vs. Pulse Width		2ns to 23ns pulse width, relative to 12.5ns pulse width			±60		ps
Prop-Delay Dispersions vs. Slew Rate		0.5V/ns to 2V/ns			50		ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC OUTPUTS							
Reference Voltages COMPHI and COMPLO		(Note 15)		0		+3.6	V
Output High Voltage Offset		I_{OUT} = 0mA, relative to COMPHI at V_{COMPHI} = 1V				±50	mV
Output Low Voltage Offset		I_{OUT} = 0mA, relative to COMPLO at V_{COMPLO} = 0V				±50	mV
Output Resistance		$I_{CHV\_}$ = $I_{CLV\_}$ = ±10mA		40	50	60	Ω
Current Limit					25		mA
Rise/Fall Time		20% to 80%, $V_{CHV\_}$ = $1V_{P-P}$, load = T-line, 50Ω, > 1ns			0.7		ns
PASSIVE LOAD							
DC CHARACTERISTICS ($R_{DUT\_}$ ≥ 10MΩ)							
LDV_ Voltage Range				-2.2		+5.2	V
Gain				0.99		1.01	V/V
Gain Temperature Coefficient					0.02		%/°C
Offset						±100	mV
Offset Temperature Coefficient					0.02		mV/°C
Power-Supply Rejection Ratio	PSRR				10		mV/V
Output Resistance Tolerance—High Value		$I_{DUT\_}$ = ±0.2mA, $V_{LDV\_}$ = 1.5V	A grade	7.125	7.5	7.875	kΩ
			B grade	4.200	6.0	7.875	
Output Resistance Tolerance—Low Value		$I_{DUT\_}$ = ±0.1mA, $V_{LDV\_}$ = 1.5V	A grade	1.90	2.0	2.10	kΩ
			B grade	1.05	1.5	2.10	
Switch Resistance Variation		Relative to 1.5V	0 to 3V		±10		%
			Full range		±30		
Maximum Output Current (Note 16)		$V_{LDV\_}$ = -2V, $V_{DUT\_}$ = +5V			±4		mA
		$V_{LDV\_}$ = +5V, $V_{DUT\_}$ = -2V			±4		
Linearity Error, Full Range		Measured at -2.2V, +1.5V, and +5.2V (Note 16)				±25	mV
AC CHARACTERISTICS							
Settling Time, LDV_ to Output		$V_{LDV\_}$ = -2V to +5V step, $R_{DUT\_}$ = 100kΩ (Note 17)			0.5		µs
Output Transient Response		$V_{LDV\_}$ = +1.5V, $V_{DUT\_}$ = -2V to +5V square wave at 1MHz, $R_{DUT\_}$ = 50Ω			20		ns

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMU SWITCHES (FORCE_, SENSE_, PMU_)						
Voltage Range			-2.2		+5.2	V
Force Switch Resistance		$V_{FORCE\_}$ = 1.5V, $I_{PMU\_}$ = ±10mA			40	Ω
Force Switch Compliance		$V_{PMU\_}$ = 6.2V, $V_{FORCE\_}$ set to make $I_{FORCE\_}$ = 30mA	25			mA
		$V_{PMU\_}$ = -3.2V, $V_{FORCE\_}$ set to make $I_{FORCE\_}$ = -30mA	25			
Force Switch Resistance Variation (Note 18)		0 to 3V		±10		%
		Full range		±30		
Sense Switch Resistance			700	1000	1300	Ω
Sense Switch Resistance Variation		Relative to 1.3V, full range		±30		%
PMU_ Capacitance		Force-and-sense switches open		5		pF
FORCE_ Capacitance				5		pF
SENSE_ Capacitance				0.2		pF
FORCE_ External Capacitance		Allowable external capacitance		2		nF
SENSE_ External Capacitance		Allowable external capacitance		1		nF
FORCE_ and SENSE_ Switching Speed		Connect or disconnect		10		µs
PMU_ Leakage		FORCE EN_ = SENSE EN_ = 0, $V_{FORCE\_}$ = $V_{SENSE\_}$ = -2.2V to +5.2V		±0.5	±5	nA
TOTAL FUNCTION						
DUT_						
Leakage, High-Impedance Mode		Load switches open, $V_{DUT\_}$ = +5.2V, $V_{CLV\_}$ = $V_{CHV\_}$ = -2.2V, $V_{DUT\_}$ = -2.2V, $V_{CLV\_}$ = $V_{CHV\_}$ = +5.2V, full range			2	µA
Leakage, Low-Leakage Mode		Full range		±1	±20	nA
Low-Leakage Recovery Time		(Note 19)		10		µs
Combined Capacitance		Term mode		2		pF
		High-impedance mode		5		
Load Resistance		(Note 20)		1		GΩ
Load Capacitance		(Note 20)		12		nF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE INPUTS (DHV_, DTV_, DLV_, DATA_, RCV_, CHV_, CLV_, LDV_, COMPHI, COMPLO)						
Input Bias Current					±100	µA
Input Bias Current Temperature Coefficient				±200		nA/°C
Settling to Output		0.1% of full-scale step		10		µs
DIGITAL INPUTS (DATA_, RCV_, $\overline{LD}$, DIN, SCLK, $\overline{CS}$)						
Input High Voltage		(Note 21)	V_L / 2 + 0.2		+3.6	V
Input Low Voltage		(Note 21)	-0.3		V_L / 2 - 0.2	V
Input Bias Current					100	µA
SERIAL DATA OUTPUT (DOUT)						
Output High Voltage		I_{OH} = -1mA	V_L - 0.4		V_L	V
Output Low Voltage		I_{OL} = 1mA	0		+0.4	V
Output Rise and Fall Time		C_L = 10pF		1.1		ns
SCLK to DOUT Delay		C_L = 10pF	t_{DH}		t_{SCLK} - t_{DS} - 2ns	ns
SERIAL-INTERFACE TIMING (Note 22)						
SCLK Frequency					50	MHz
SCLK Pulse-Width High	t_{CH}		10			ns
SCLK Pulse-Width Low	t_{CL}		10			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}		0			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		15			ns
DIN to SCLK High Setup	t_{DS}		3.5			ns
DIN to SCLK High Hold	t_{DH}		1			ns
$\overline{CS}$ High to $\overline{LOAD}$ Low Setup	t_{CLL}		6			ns
$\overline{LD}$ Low Hold Time	t_{LDW}		5			ns
$\overline{LD}$ High to Any Activity			0			ns
V_L Rising to $\overline{CS}$ Low		Power-on delay		2		µs
TEMP SENSOR						
Nominal Voltage		T_J = +27°C		3.00		V
Temperature Coefficient				+10		mV/°C
Output Resistance				500		Ω

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

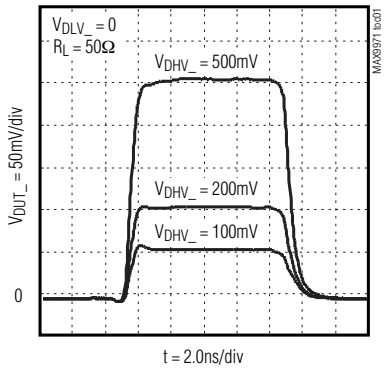
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	(Note 23)	7.6	8	8.4	V
Negative Supply Voltage	V_{SS}	(Note 23)	-5.25	-5	-4.75	V
Logic Supply Voltage	V_L		2.3		3.6	V
Positive Supply Current	I_{DD}	f_{OUT} = 0MHz		97	120	mA
Negative Supply Current	I_{SS}	f_{OUT} = 0MHz		99	120	mA
Logic Supply Current	I_L			0.15	0.30	mA
Static Power Dissipation		f_{OUT} = 0MHz		1.3	1.5	W
Operating Power Dissipation		f_{OUT} = 100Mbps (Note 24)		1.4		W

Note 1: All minimum and maximum specifications are 100% production tested except driver dynamic output current, which is guaranteed by design. All specifications are with DUT_ and PMU_ electrically isolated, unless otherwise noted.
Note 2: Nominal target value is 49.5Ω. Contact factory for alternate trim selections within the 45Ω to 55Ω range.
Note 3: Measured at 1.5V, relative to a straight line through 0 and 3V.
Note 4: Measured at end points, relative to a straight line through 0 and 3V.
Note 5: DUT_ is terminated with 50Ω to ground, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, unless otherwise specified. DATA_ and RCV_ logic levels are V_{HIGH} = 2V, V_{LOW} = 1V.
Note 6: Undershoot is any reflection of the signal back towards its starting voltage after it has reached 90% of its swing. Preshoot is any aberration in the signal before it reaches 10% of its swing.
Note 7: At the minimum voltage swing, undershoot is less than 20%. DHV_ and DLV_ references are adjusted to result in the specified swing.
Note 8: At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.
Note 9: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.
Note 10: Relative to a straight line through 0 and 3V.
Note 11: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to 1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V, t_R = t_F = 500ps, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = +0.5V. Comparator outputs are terminated with 50Ω to GND. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to midpoint of nominal comparator output swing.
Note 12: Terminated is defined as driver in drive mode and set to zero volts.
Note 13: High impedance is defined as driver in high-impedance mode.
Note 14: $V_{DUT\_}$ = 200mV_{P-P}. Propagation delay is compared to a reference time at 1.5V.
Note 15: The comparator meets all its timing specifications with the specified output conditions when the output current is less than 15mA, V_{COMPHI} > V_{COMPLO}, and V_{COMPHI} - V_{COMPLO} ≤ 1V. Higher voltage swings are valid but AC performance may degrade.
Note 16: LOAD EN LOW = LOAD EN HIGH = 1.
Note 17: Waveform settles to within 5% of final value into load 100kΩ.
Note 18: $I_{PMU\_}$ = ±2mA at $V_{FORCE\_}$ = -2.2V, +1.5V, and +5.2V. Percent variation relative to value calculated at $V_{FORCE\_}$ = +1.5V.
Note 19: Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_.
Note 20: Load at end of 2ns transmission line; for stability only, AC performance may be degraded.
Note 21: The driver meets all of its timing specifications over the specified digital input voltage range.
Note 22: Timing characteristics with V_{LOGIC} = 3V.
Note 23: Specifications are simulated and characterized over the full power-supply range. Production tests are performed with power supplies at typical values.
Note 24: All channels driven at 3V_{P-P}, load = 2ns, 50Ω transmission line terminated with 3pF.

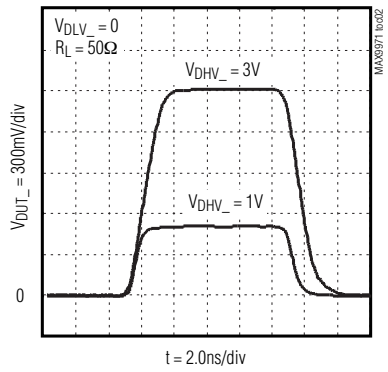
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

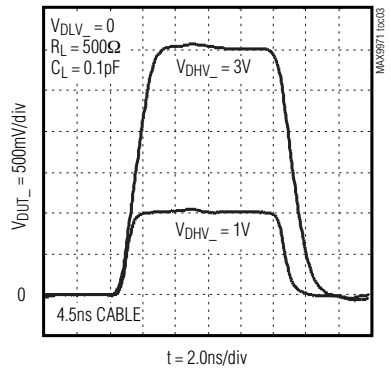
DRIVER SMALL-SIGNAL RESPONSE



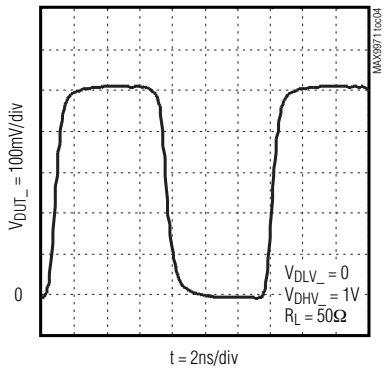
DRIVER LARGE-SIGNAL RESPONSE



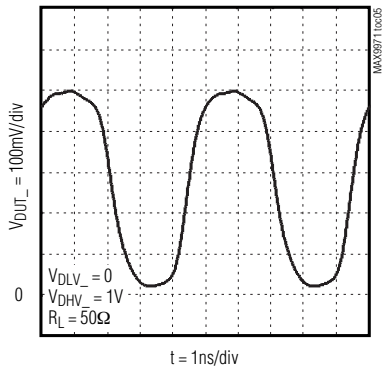
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



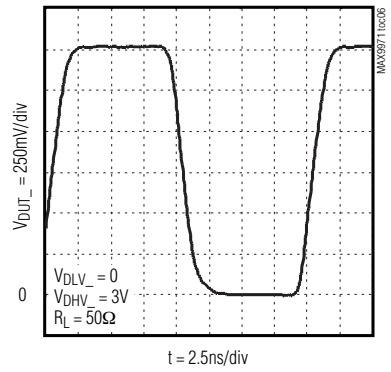
DRIVER 1VP-P, 150Mbps SIGNAL RESPONSE



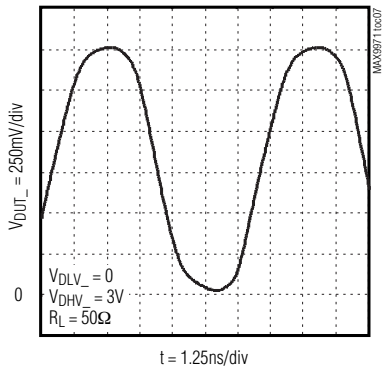
DRIVER 1VP-P, 400Mbps SIGNAL RESPONSE



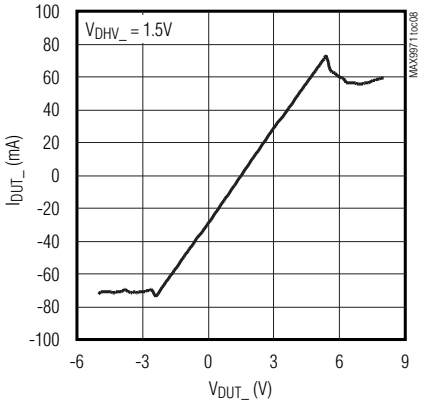
DRIVER 3VP-P, 100Mbps SIGNAL RESPONSE



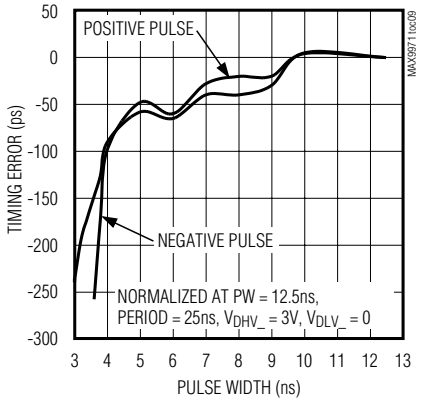
DRIVER 3VP-P, 250Mbps SIGNAL RESPONSE



DRIVER DC CURRENT-LIMIT AND OVERVOLTAGE RESPONSE



DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH

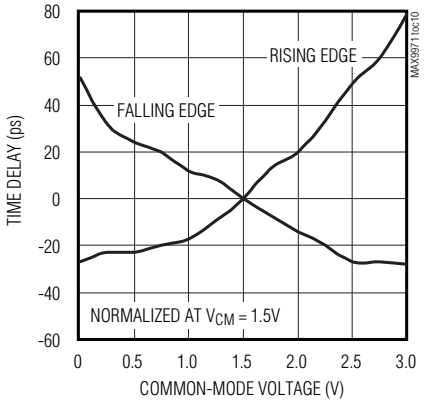


Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

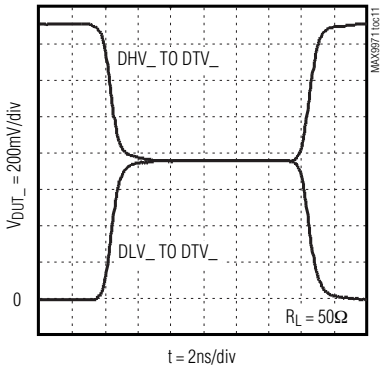
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

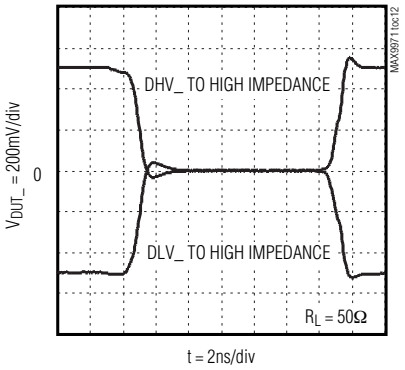
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



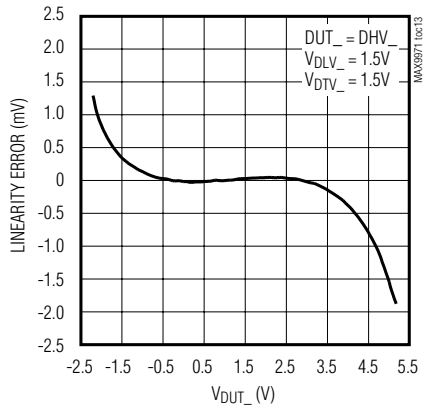
DRIVE-TO-TERM TRANSITION



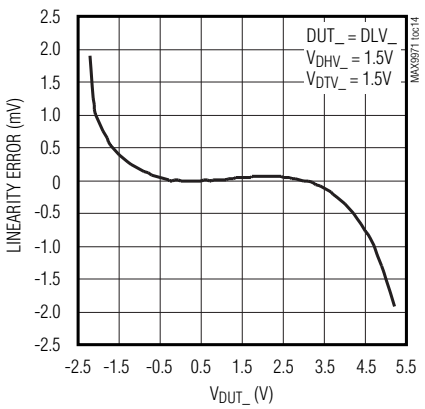
DRIVE-TO-HIGH-IMPEDANCE TRANSITION



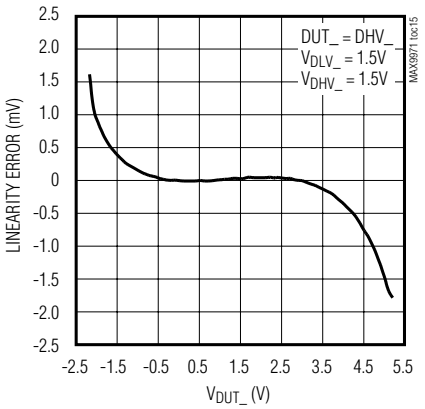
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



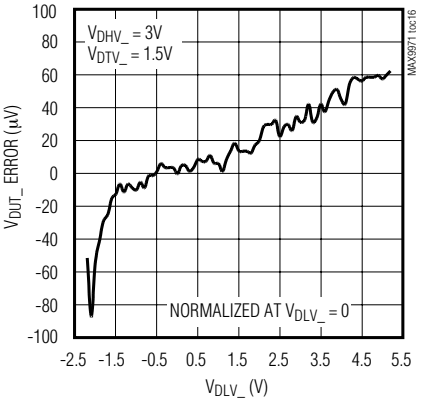
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



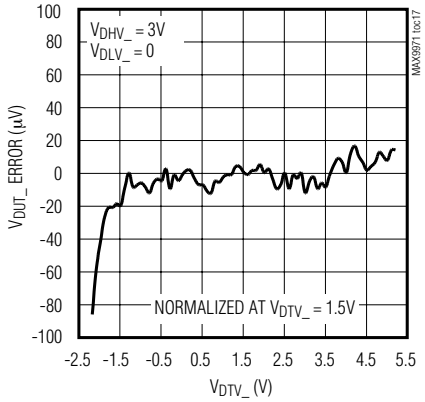
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



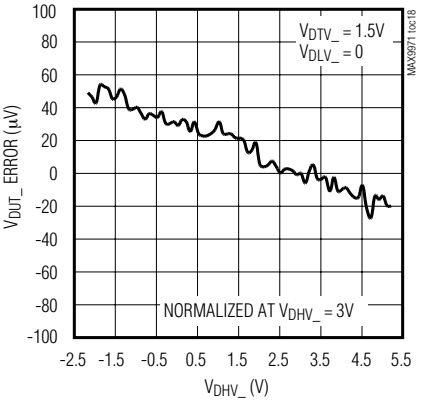
CROSSTALK, DUT_ DRIVEN BY DHV_ WITH DLV_ VARIED



CROSSTALK, DUT_ DRIVEN BY DHV_ WITH DTV_ VARIED



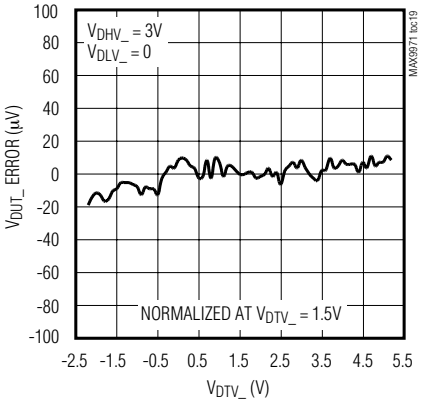
CROSSTALK, DUT_ DRIVEN BY DLV_ WITH DHV_ VARIED



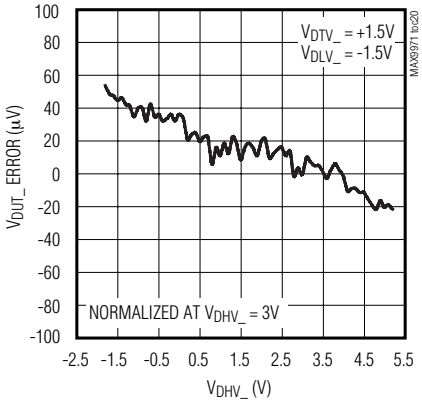
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

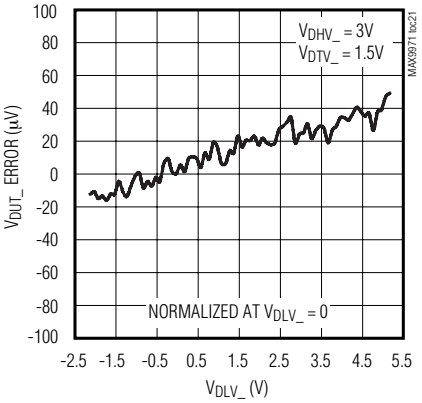
CROSSTALK, DUT_ DRIVEN BY DLV_ WITH DTV_ VARIED



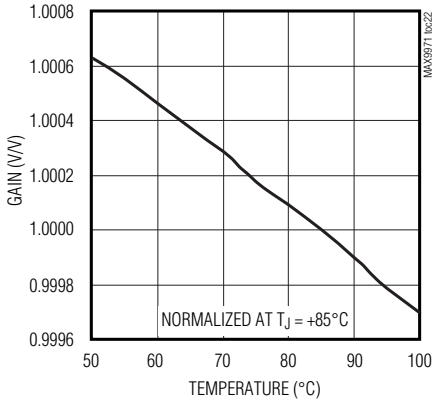
CROSSTALK, DUT_ DRIVEN BY DTV_ WITH DHV_ VARIED



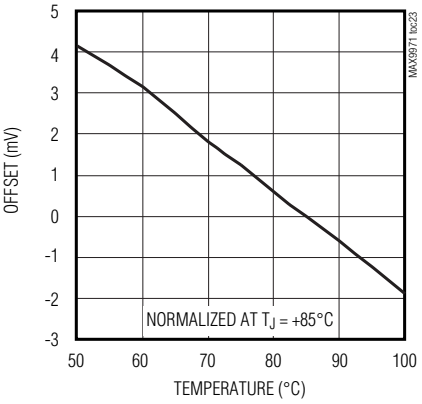
CROSSTALK, DUT_ DRIVEN BY DTV_ WITH DLV_ VARIED



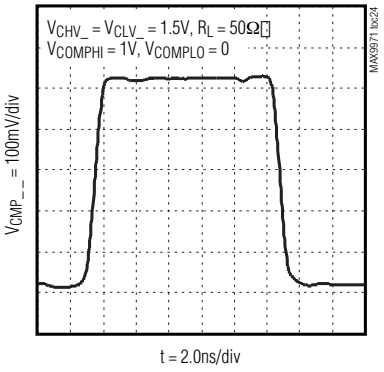
DRIVER GAIN vs. TEMPERATURE



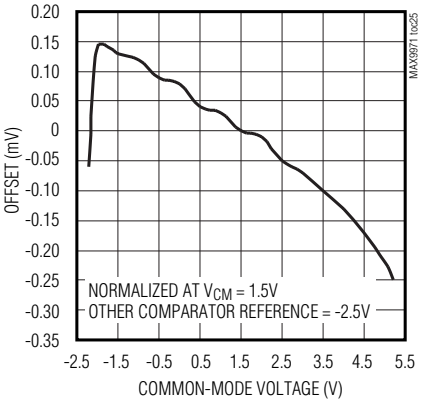
DRIVER OFFSET vs. TEMPERATURE



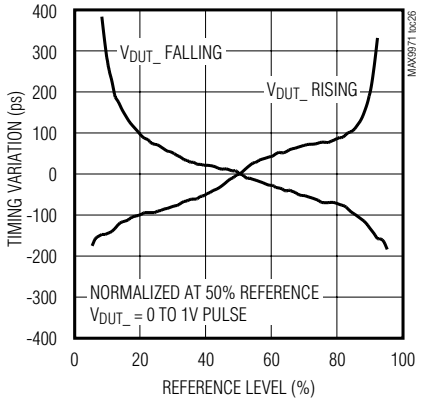
COMPARATOR RESPONSE TO 0 TO 3V SIGNAL



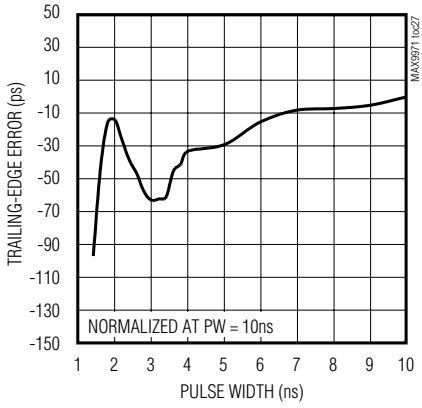
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



COMPARATOR WAVEFORM TRACKING



COMPARATOR TIMING VARIATION vs. PULSE WIDTH

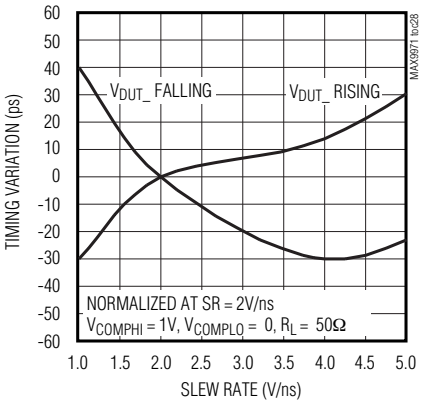


Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

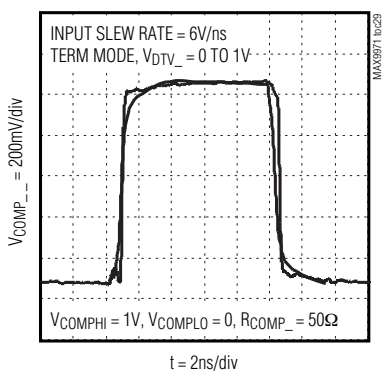
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

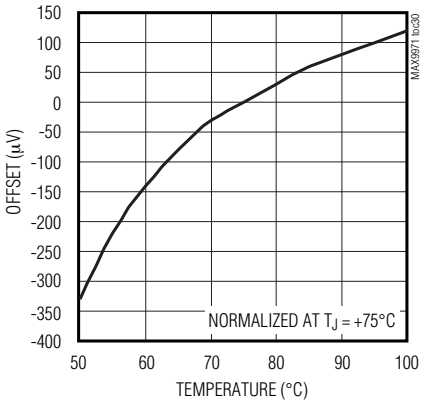
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE



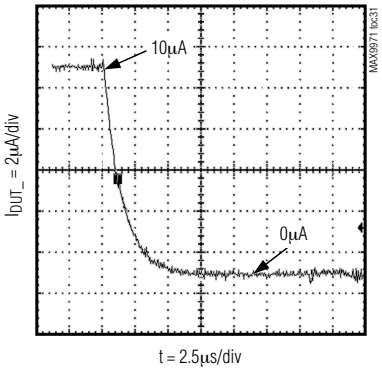
COMPARATOR RESPONSE vs. HIGH SLEW-RATE OVERDRIVE



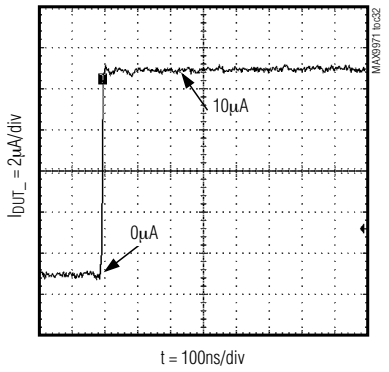
COMPARATOR OFFSET vs. TEMPERATURE



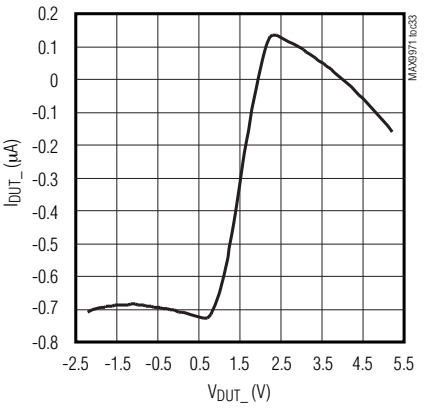
DRIVE 1V TO LOW-LEAKAGE TRANSITION



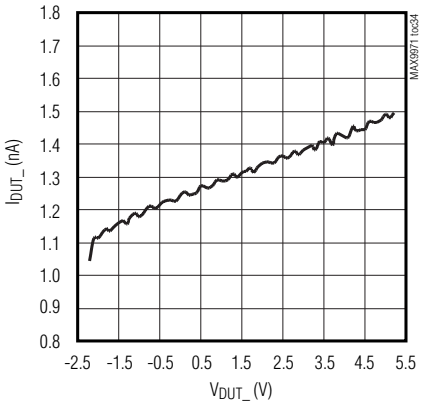
LOW LEAKAGE TO DRIVE 1V TRANSITION



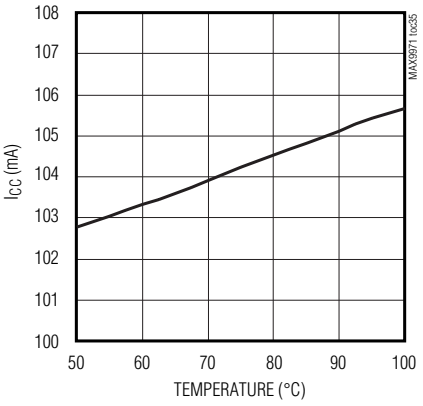
HIGH-IMPEDANCE LEAKAGE AT DUT_ vs. DUT_ VOLTAGE



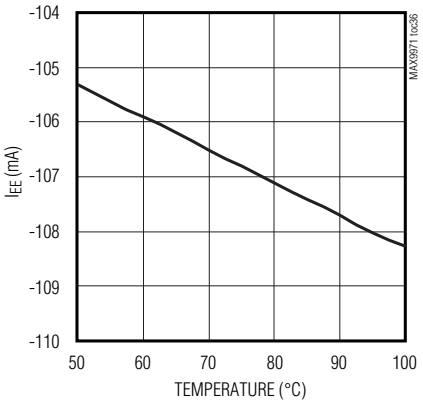
LOW-LEAKAGE CURRENT vs. DUT_VOLTAGE



ICC SUPPLY CURRENT vs.TEMPERATURE



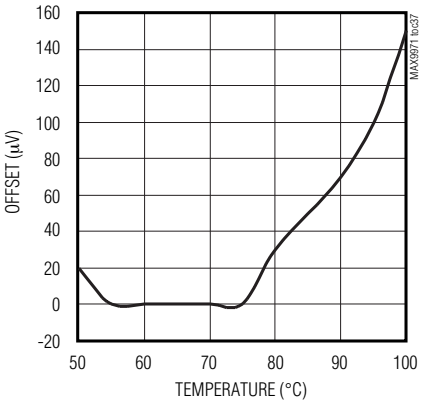
IEE SUPPLY CURRENT vs.TEMPERATURE



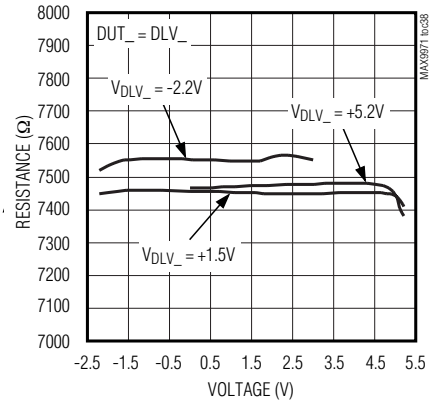
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

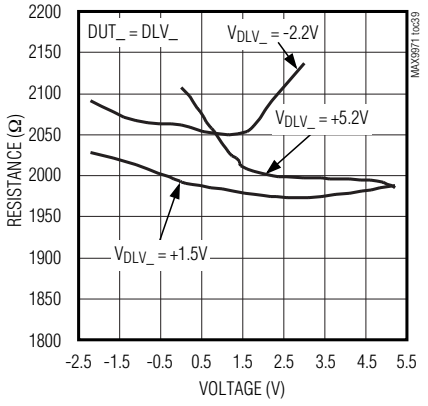
PASSIVE LOAD OFFSET vs. TEMPERATURE



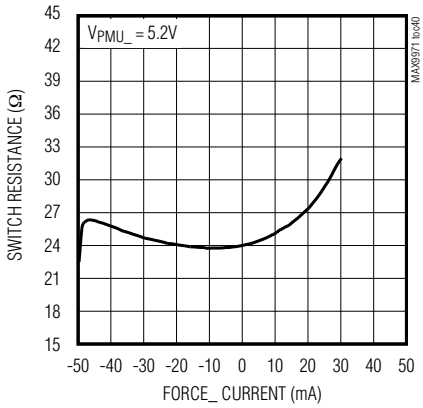
PASSIVE LOAD HIGH RESISTOR vs. VOLTAGE



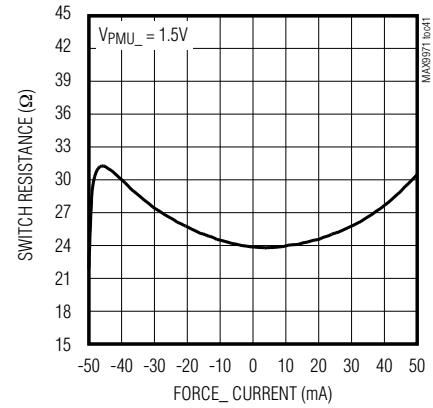
PASSIVE LOAD LOW RESISTOR vs. VOLTAGE



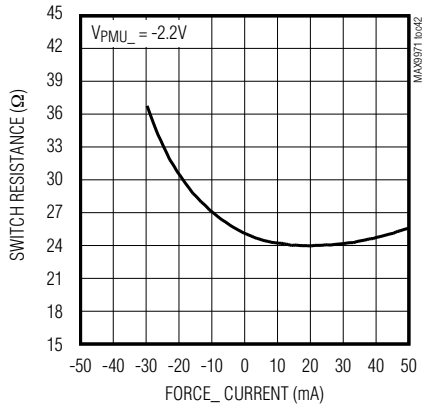
PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

Pin Description

PIN		NAME	FUNCTION
MAX9972	MAX9971		
1	60	DATA1	Channel 1 Multiplexer Control Input. Selects driver 1 input from DHV1 or DLV1 in drive mode. See Table 1 and Figure 2.
2	59	RCV1	Channel 1 Multiplexer Control Input. Sets channel 1 mode to drive or receive. See Table 1 and Figure 2.
3, 8, 13, 18, 51	10, 43, 48, 53, 58	GND	Analog Ground
4	57	CMPH1	Channel 1 High-Side Comparator Output
5	56	CMPL1	Channel 1 Low-Side Comparator Output
6	55	DATA2	Channel 2 Multiplexer Control Input. Selects driver 2 input from DHV2 or DLV2 in drive mode. See Table 1 and Figure 2.
7	54	RCV2	Channel 2 Multiplexer Control Input. Sets channel 2 mode to drive or receive. See Table 1 and Figure 2.
9	52	CMPH2	Channel 2 High-Side Comparator Output
10	51	CMPL2	Channel 2 Low-Side Comparator Output
11	50	CMPL3	Channel 3 Low-Side Comparator Output
12	49	CMPH3	Channel 3 High-Side Comparator Output
14	47	RCV3	Channel 3 Multiplexer Control Input. Sets channel 3 mode to drive or receive. See Table 1 and Figure 2.
15	46	DATA3	Channel 3 Multiplexer Control Input. Selects driver 3 input from DHV3 or DLV3 in drive mode. See Table 1 and Figure 2.
16	45	CMPL4	Channel 4 Low-Side Comparator Output
17	44	CMPH4	Channel 4 High-Side Comparator Output
19	42	RCV4	Channel 4 Multiplexer Control Input. Sets channel 4 mode to drive or receive. See Table 1 and Figure 2.
20	41	DATA4	Channel 4 Multiplexer Control Input. Selects driver 4 input from DHV4 or DLV4 in drive mode. See Table 1 and Figure 2.
21	40	DHV4	Channel 4 Driver High Voltage Input
22	39	DLV4	Channel 4 Driver Low Voltage Input
23	38	DTV4	Channel 4 Driver Termination Voltage Input
24	37	CHV4	Channel 4 Threshold Voltage Input for High-Side Comparator
25	36	CLV4	Channel 4 Threshold Voltage Input for Low-Side Comparator
26	35	DHV3	Channel 3 Driver High Voltage Input
27	34	DLV3	Channel 3 Driver Low Voltage Input
28	33	DTV3	Channel 3 Driver Termination Voltage Input
29	32	CHV3	Channel 3 Threshold Voltage Input for High-Side Comparator
30	31	CLV3	Channel 3 Threshold Voltage Input for Low-Side Comparator
31	30	DGND	Digital Ground Connection
32	29	DOUT	Serial-Interface Data Output
33	28	$\overline{LD}$	Load Input. Latches data from the serial input register to the control register on rising edge. Transparent when low.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9972	MAX9971		
34	27	DIN	Serial-Interface Data Input
35	26	SCLK	Serial Clock
36	25	$\overline{CS}$	Chip Select
37	24	SENSE4	Channel 4 PMU Sense Connection
38	23	FORCE4	Channel 4 PMU Force Connection
39	22	SENSE3	Channel 3 PMU Sense Connection
40	21	FORCE3	Channel 3 PMU Force Connection
41	20	TEMP	Temperature Sensor Output
42, 47, 52, 56, 60	1, 5, 9, 14, 19	V_{DD}	Positive Power-Supply Input
43	18	DUT4	Channel 4 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 4.
44	17	PMU4	Channel 4 Parametric Measurement Connection. PMU switch I/O node for channel 4.
45, 50, 53, 57	4, 8, 11, 16	V_{SS}	Negative Power-Supply Input
46	15	V_L	Logic Power-Supply Input
48	13	DUT3	Channel 3 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 3.
49	12	PMU3	Channel 3 Parametric Measurement Connection. PMU switch I/O node for channel 3.
54	7	PMU2	Channel 2 Parametric Measurement Connection. PMU switch I/O node for channel 2.
55	6	DUT2	Channel 2 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 2.
58	3	PMU1	Channel 1 Parametric Measurement Connection. PMU switch I/O node for channel 1.
59	2	DUT1	Channel 1 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 1.
61	80	FORCE2	Channel 2 PMU Force Connection
62	79	SENSE2	Channel 2 PMU Sense Connection
63	78	FORCE1	Channel 1 PMU Force Connection
64	77	SENSE1	Channel 1 PMU Sense Connection
65	76	COMPLO	Comparator Output-Low Voltage Reference Input
66	75	COMPHI	Comparator Output-High Voltage Reference Input
67	74	LDV4	Channel 4 Load Voltage Input
68	73	LDV3	Channel 3 Load Voltage Input
69	72	LDV2	Channel 2 Load Voltage Input
70	71	LDV1	Channel 1 Load Voltage Input
71	70	CLV2	Channel 2 Threshold Voltage Input for Low-Side Comparator
72	69	CHV2	Channel 2 Threshold Voltage Input for High-Side Comparator
73	68	DTV2	Channel 2 Driver Termination Voltage Input
74	67	DLV2	Channel 2 Driver Low Voltage Input
75	66	DHV2	Channel 2 Driver High Voltage Input
76	65	CLV1	Channel 1 Threshold Voltage Input for Low-Side Comparator
77	64	CHV1	Channel 1 Threshold Voltage Input for High-Side Comparator
78	63	DTV1	Channel 1 Driver Termination Voltage Input
79	62	DLV1	Channel 1 Driver Low Voltage Input
80	61	DHV1	Channel 1 Driver High Voltage Input
—	—	EP	Exposed Pad. Leave unconnected or connect to V_{SS}.

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

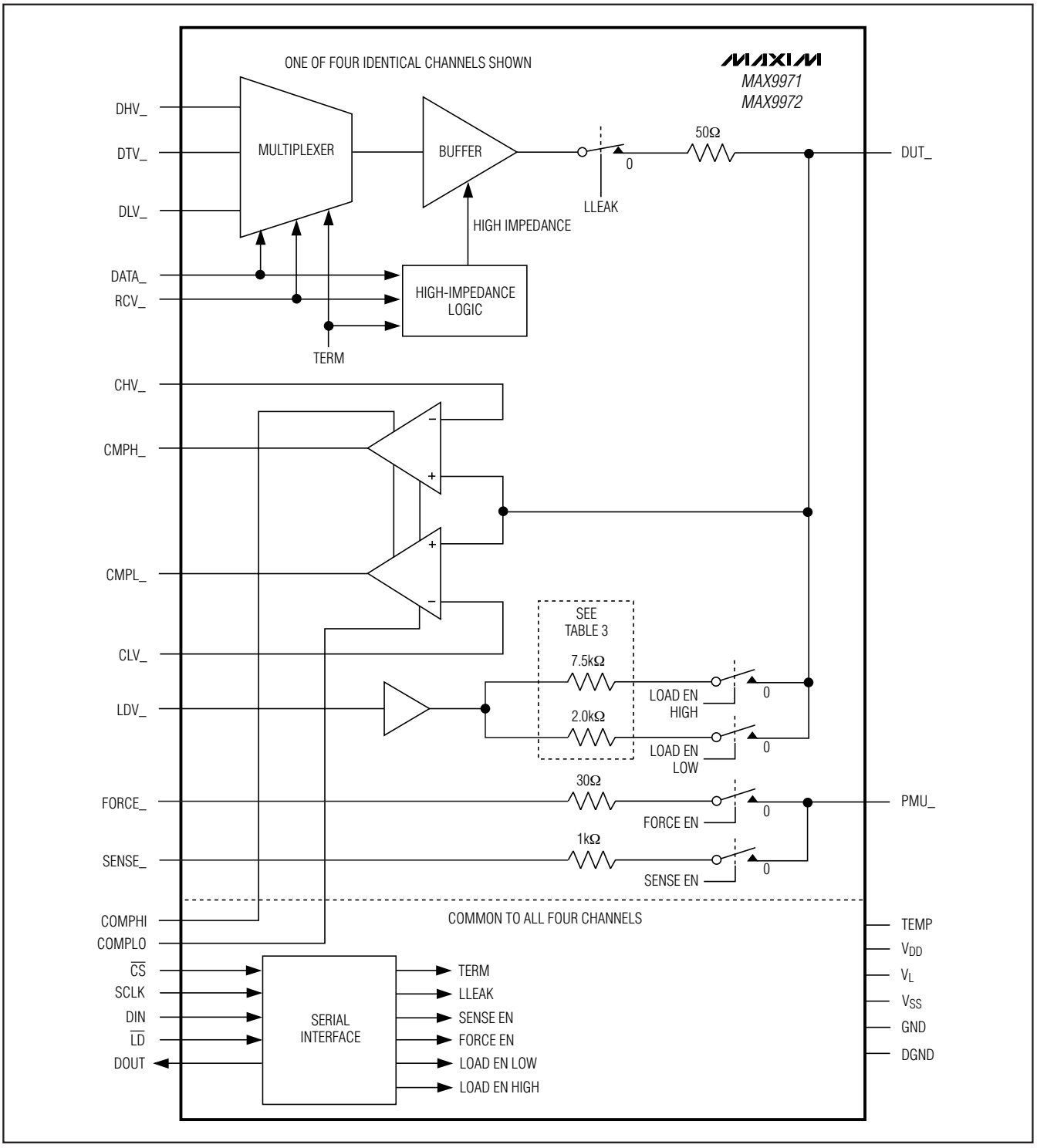


Figure 1. Block Diagram

Detailed Description

The MAX9971/MAX9972 are four-channel, pin-electronics ICs for automated test equipment that include, for each channel, a three-level pin driver, a window comparator, a passive load, and a Kelvin instrument connection (Figure 1). All functions feature a -2.2V to +5.2V operating range and the drivers include both high-impedance and active-termination (3rd-level drive) modes. The comparators feature programmable output voltages, allowing optimization for different CMOS interface standards. The loads have selectable output resistance for optimizing DUT current loading. The Kelvin paths allow accurate connection of an instrument with ±25mA source/sink capability. Additionally, the MAX9971/MAX9972 offer a low-leakage mode that reduces DUT_ leakage current to less than 20nA.

The MAX9971/MAX9972 are available in two grades. The A-grade devices provide tighter tolerances for driver gains and offsets, comparator offsets, and load resistor values. This allows reference levels to be shared across multiple channels in cost-sensitive systems. The B-grade devices are intended for system designs that incorporate independent reference levels for each channel.

Each of the four channels feature single-ended CMOS-compatible inputs, DATA_ and RCV_, for control of the driver signal path (Figure 2). The MAX9971/MAX9972 modal operation is programmed through a 3-wire, low-voltage CMOS-compatible serial interface.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs; DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_, and mode-control bit TERM (Table 1). DATA_ and RCV_ are single-ended inputs with threshold levels equal to V_L / 2. Each channel's threshold levels are independently generated to minimize crosstalk.

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). High-speed input RCV_ and mode-control bits TERM and LLEAK control these modes. In high-impedance mode, the bias current at DUT_ is less than 2µA over the -2.2V to +5.2V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 20nA, and signal tracking slows.

The nominal driver output resistance is 50Ω. Custom resistance values from 45Ω to 51Ω are possible; consult factory for further information.

Table 1. Driver Channel Control Signals

EXTERNAL CONNECTIONS		INTERNAL CONTROL BITS		DRIVER OUTPUT	DRIVER MODE
RCV_	DATA_	TERM	LLEAK		
0	0	X	0	DUT_ = DLV_	Drive
0	1	X	0	DUT_ = DHV_	Drive
1	X	0	0	High Impedance	Receive
1	X	1	0	DUT_ = DTV_	Receive
X	X	X	1	Low Leak	Low Leakage

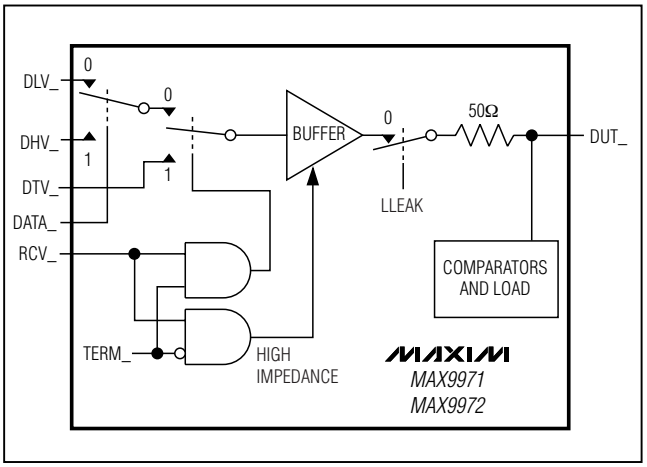


Figure 2. Multiplexer and Driver Channel

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

Comparators

The MAX9971/MAX9972 provide two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (see Figure 1). Comparator outputs are a logical result of the input conditions, as indicated in Table 2.

The comparator output voltages are easily interfaced to a wide variety of logic standards. Use buffered inputs COMPHI and COMPLO to set the high and low output voltages. For correct operation, COMPHI should be greater than or equal to COMPLO. The comparator 50Ω output impedance provides source termination (Figure 3).

Passive Load

The MAX9971/MAX9972 channels each feature a passive load consisting of a buffered input voltage, LDV_, connected to DUT_ through two resistive paths (Figure 1). Each path connects to DUT_ individually by a switch controlled through the serial interface. Programming options include none (load disconnected), either, or both paths connected. The resistor values vary depending on the accuracy grade of the device, as shown in Table 3. The loads facilitate fast open/short testing in conjunction with the comparator, and pullup of open-drain DUT_ outputs.

Parametric Switches

Each of the four MAX9971/MAX9972 channels provides force-and-sense paths for connection of a PMU or other DC resource to the device-under-test (Figure 1). Each force-and-sense switch is independently controlled though the serial interface providing maximum application flexibility. PMU_ and DUT_ are provided on separate pins allowing designs that do not require the parametric switch feature to avoid the added capacitance of PMU_. It also allows PMU_ to connect to DUT_ either directly or with an impedance-matching network.

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port places the MAX9971/MAX9972 into a very-low-leakage state (see the *Electrical Characteristics* table). This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK control is independent for each channel.

When DUT_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Table 2. Comparator Logic

DUT_ > CHV_	DUT_ > CLV_	CMPH_	CMPL_
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

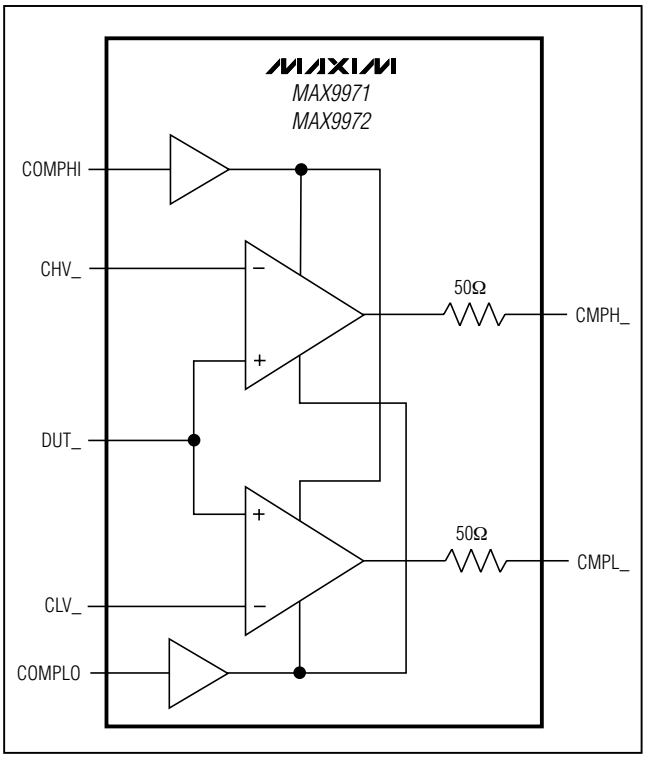


Figure 3. Complementary 50Ω Comparator Outputs

Table 3. Passive Load Resistance Values

ACCURACY GRADE	HIGH RESISTOR (kΩ)	LOW RESISTER (kΩ)
A	7.5	2
B	6	1.5

Temperature Monitor

Each device supplies a single temperature output signal, TEMP, that asserts a nominal 3.43V output voltage at a +70°C (343K) die temperature. The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 500Ω, typical.

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9971/MAX9972 modes (Figure 4). Control data flow into a 12-bit shift register (MSB first) and are latched when $\overline{CS}$ is taken high. Data from the shift register are then loaded to the per-channel control latches as determined by bits D8–D11, and indicated in Figure 4 and Table 4. The latches contain the six mode bits for each channel of the device. The mode bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel. Transfer data asynchronously from the input registers to the channel registers by forcing $\overline{LD}$ low. With $\overline{LD}$ always low, data transfer on the rising edge of $\overline{CS}$.

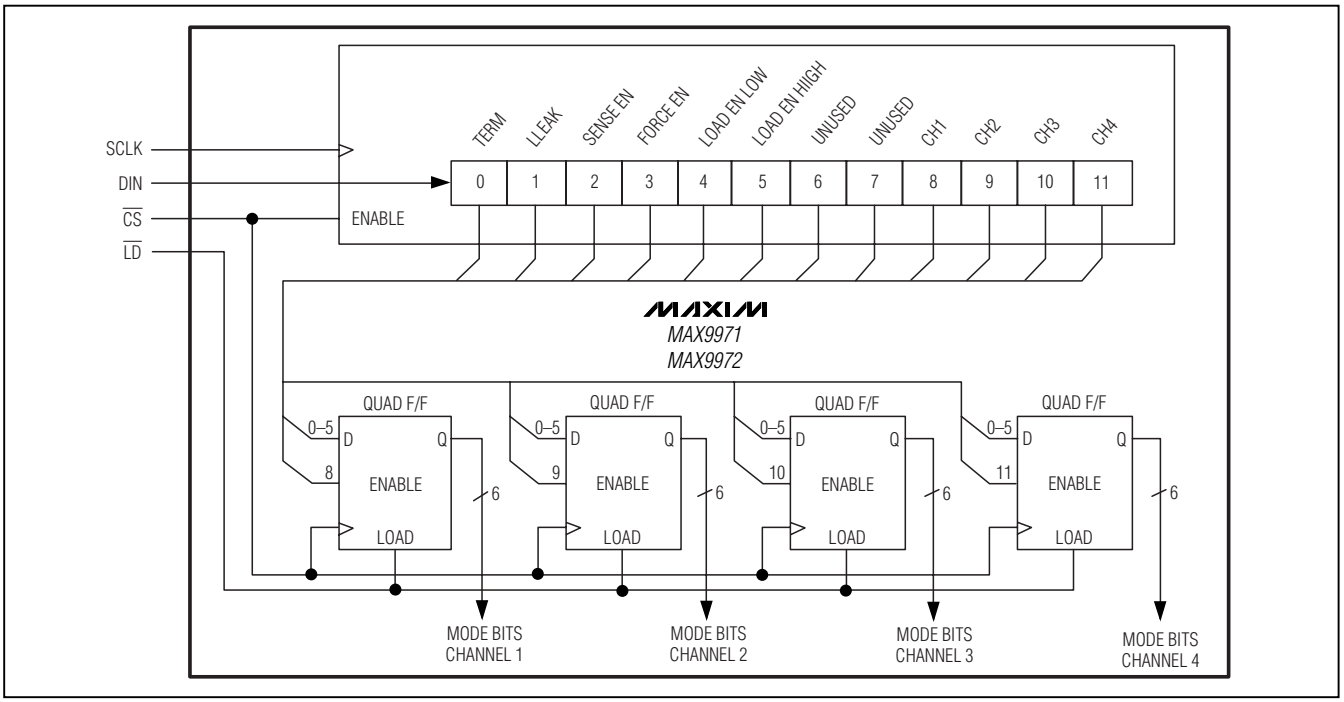


Figure 4. Serial Interface

Table 4. Control Register Bit Functions

BIT	NAME	FUNCTION	BIT STATE		POWER-UP STATE
			0	1	
0	TERM	Term Mode Control	High Impedance	Term Mode	0
1	LLEAK	Assert Low-Leakage Mode	Term Mode	Low Leakage	0
2	SENSE EN	Enable Sense Switch	Disabled	Enabled	0
3	FORCE EN	Enable Force Switch	Disabled	Enabled	0
4	LOAD EN LOW	Enable Low Load Resistor	Disabled	Enabled	0
5	LOAD EN HIGH	Enable High Load Resistor	Disabled	Enabled	0
6	—	Unused	X	X	0
7	—	Unused	X	X	0
8	CH1	Update Channel 1 Control Register	Disabled	Enabled	1
9	CH2	Update Channel 2 Control Register	Disabled	Enabled	1
10	CH3	Update Channel 3 Control Register	Disabled	Enabled	1
11	CH4	Update Channel 4 Control Register	Disabled	Enabled	1

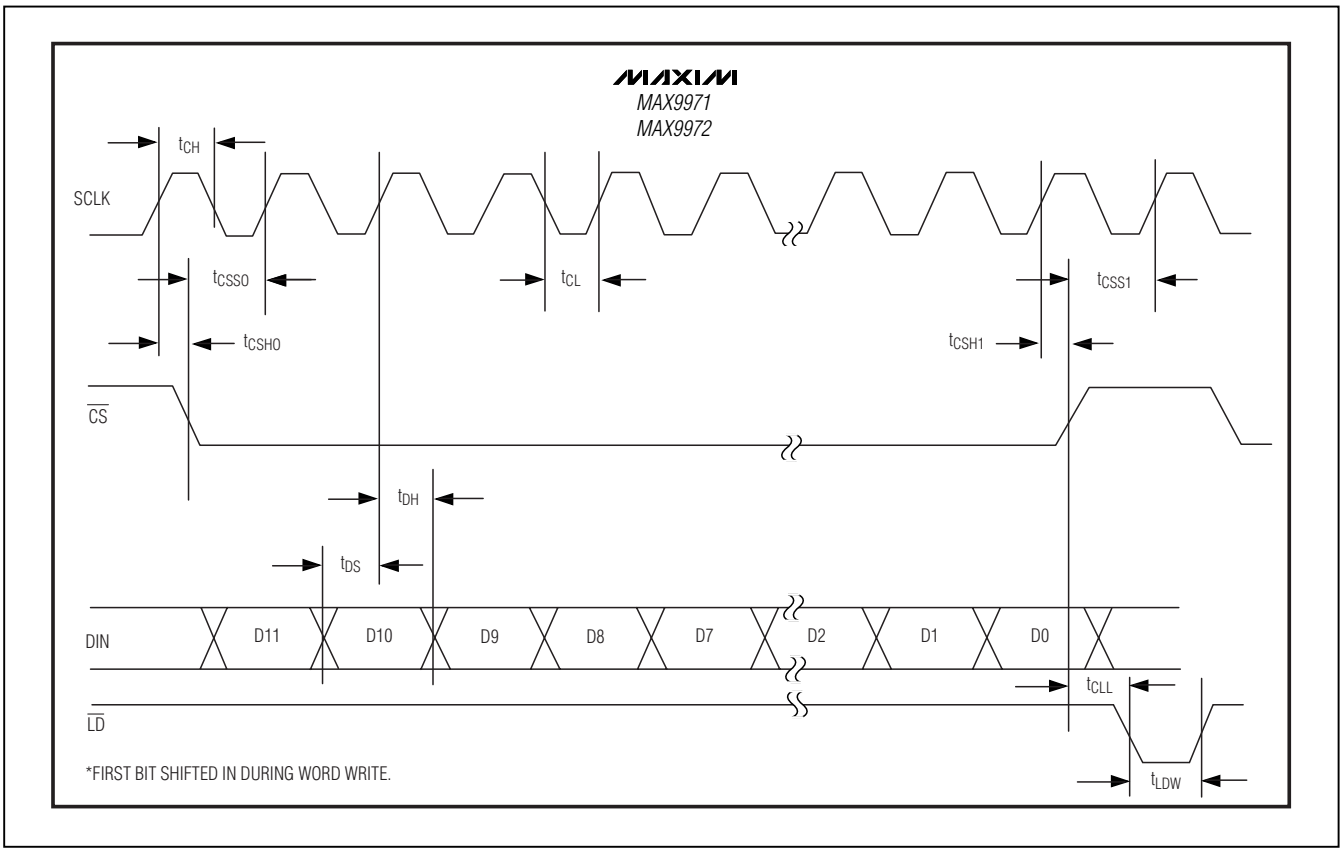


Figure 5. Serial-Interface Timing

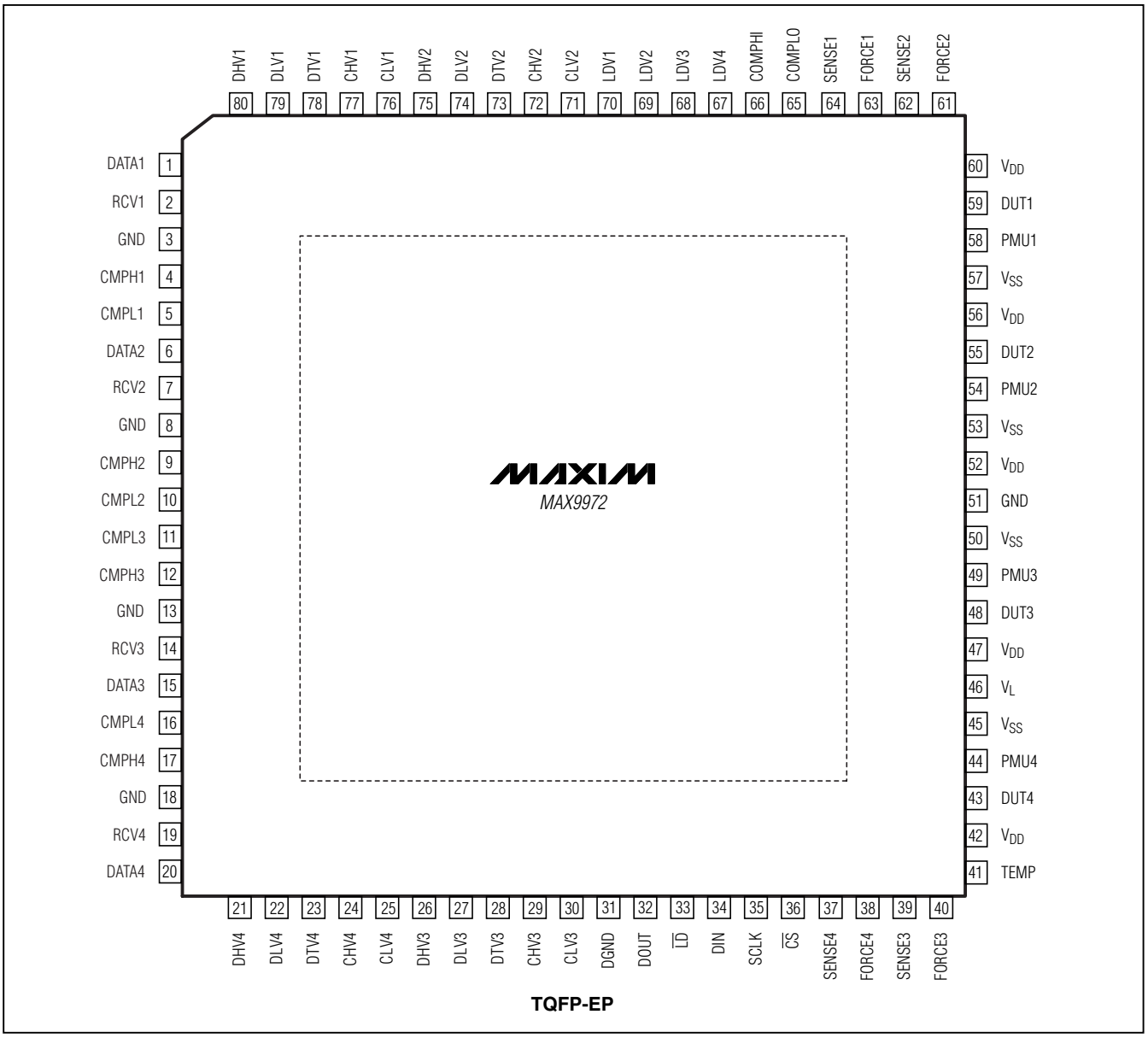
Heat Removal

With adequate airflow, no external heat sinking is needed under most operating conditions. If excess heat must be dissipated through the exposed paddle, solder it to circuit board copper (MAX9972) or use an external heat sink (MAX9971). The exposed paddle must be either left unconnected, isolated, or connected to V_{SS}.

Power Minimization

To minimize power consumption, activate only the needed channels. Each channel placed in low-leakage mode saves approximately 240mW.

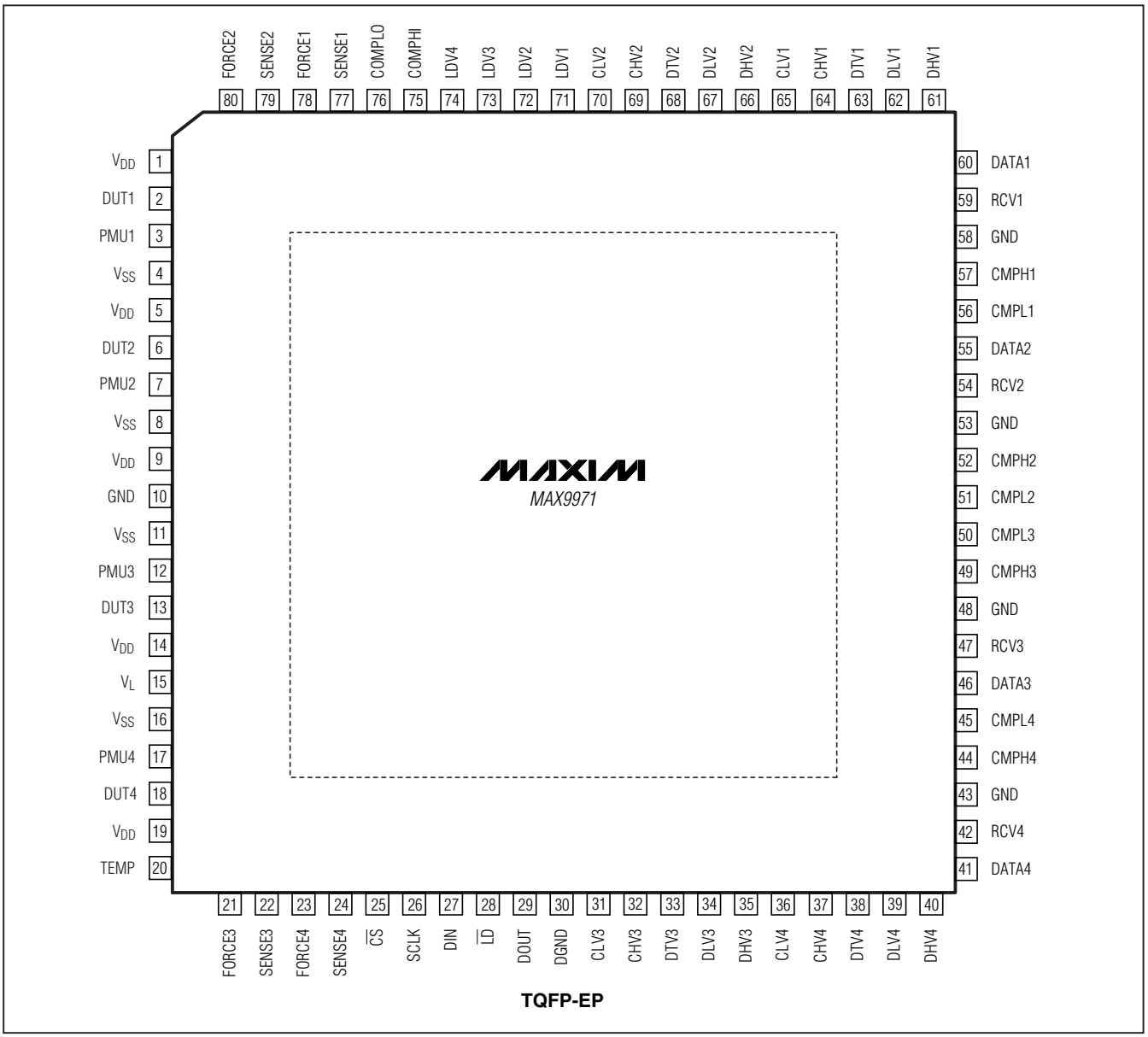
Pin Configurations



TQFP-EP

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

Pin Configurations (continued)



TQFP-EP

Chip Information

TRANSISTOR COUNT: 5728

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

TANISYS TECHNOLOGY

The Future of Test

>> see a sales sheet

M550
Flash Test System

Tanisys Continues To Lead The Way In Flash Card Test

Tanisys Technology, the leader in flash card test equipment, drives high volume Flash card manufacturing to a new level. The M550 Flash test system, built on the success of the Model 500, is designed for fully automated testing of SD, MMC, and Memory Stick Flash cards. Custom solutions for other card types or NAND device are also available. With increasing demand for NAND Flash products coupled with constant price pressure, highly parallel testing is critical. With the M550, Tanisys is setting a new standard for Flash test by providing the capability to test 320+ cards in parallel. The M550 test system offers world-class test economics while providing the highest test coverage in the industry. Tanisys test systems continue to be the choice of industry leading Flash card manufacturers worldwide.

Flexibility By Design

Tanisys Technology designed the M550 with flexibility and scalability in mind using the versatile, patented Distributed Network Architecture (DNA™). As the building block of advance parallel test solutions, DNA enables the user to seamlessly transition from engineering development to high-volume production. In combination with high-performance M550 hardware, DNA provides virtually unlimited scalability that allows the user to add capacity as needed a capability not found in other platforms.

Configurations To Meet Demand

Whether your needs are for engineering development, qualification, or volume production, the M550 test system fits the requirement. As a single or dual blade engineering system, the M550-E can be used to develop your test program in an office or lab environment. It is also the right solution for product qualification or low volume production. For high volume manufacturing requirements, the M550 is available in a multiple blade production chassis. The production test system was designed utilizing a modular approach, which allows the user to add capacity to a single system as product volume increases. The M550 test system is currently available in configurations to support 320 Flash cards with the expansion capability to support more than 640 cards.

FEATURES

- Support for SD, MMC, Memory Stick through Protocol Engines
- Complete independence between tester electronics via Tanisys' Distributed Network Architecture™
- Modular / Scalable architecture supports expansion to meet capacity needs
- Effortless migration from single site to multi-site applications
- Configurations to support from 6 to beyond 512 DUT's
- Development and Production configurations available
- Automated solutions for high volume manufacturing
- World wide support, including local applications engineering and on-site spares

Production Ready

Whether you choose your own handler or ask Tanisys to provide a turnkey solution, the M550 test system facilitates easy migration to automated environments. The M550 production configuration includes a manipulator that is designed to work with handlers from leading suppliers. With vast experience in developing handler control and production user interface software, Tanisys provides custom solutions to meet your manufacturing needs. Whatever your plan for production, the M550 is backed by Tanisys expertise and our extensive global support network.

Worldwide Support

Tanisys offers technical support to production facilities around the globe through our partnerships in Korea, Japan, Taiwan, China, Singapore and Europe. Services include sales and distribution, full technical support, applications engineering, and spares coverage the same world-class, hands-on support provided to customer in North America.

19-0474; Rev 0; 6/06

MAXIM

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

General Description

The MAX9971/MAX9972 four-channel, ultra-low-power, pin-electronics ICs include, for each channel, a three-level pin driver, a window comparator, a passive load, and force-and-sense Kelvin-switched parametric measurement unit (PMU) connections. The driver features a -2.2V to +5.2V voltage range, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The window comparator features 500MHz equivalent input bandwidth and programmable output voltage levels. The passive load provides pullup and pulldown voltages to the device-under-test (DUT).

Two grade versions are available, A grade and B grade. The A-grade version provides tight gain and offset matching for the driver and comparator, allowing reference levels to be shared across multiple channels. It also provides tighter tolerance of the load resistance values. The B-grade version is for system designs that incorporate independent reference levels for each channel.

Low-leakage, high-impedance, and terminate controls are operational configurations that are programmed through a 3-wire, low-voltage, CMOS-compatible serial interface. High-speed PMU switching is realized through dedicated digital control inputs.

These devices are available in an 80-pin, 12mm x 12mm body, 1.0mm pitch TQFP with an exposed 6mm x 6mm die pad on the bottom of the package (MAX9972), and the top of the package (MAX9971), for efficient heat removal. The MAX9971/MAX9972 are specified to operate over the 0°C to +70°C commercial temperature range, and feature a die temperature monitor output.

Applications

NAND Flash Testers

DRAM Probe Testers

Low-Cost Mixed-Signal/System-on-Chip (SOC) Testers

Active Burn-In Systems

Structural Testers

Features

- ♦ **Small Footprint—Four Channels in 0.3in²**
- ♦ **Low-Power Dissipation: 325mW/Channel Typical**
- ♦ **High Speed: 300Mbps at $3V_{P-P}$**
- ♦ **-2.2V to +5.2V Operating Range**
- ♦ **Active Termination (3rd-Level Drive)**
- ♦ **Integrated PMU Switches**
- ♦ **Passive Load**
- ♦ **Low-Leak Mode: 20nA max**
- ♦ **Low Gain and Offset Error**
- ♦ **Lead-Free Package Available**

Pin Configurations appear at end of data sheet.

Ordering Information and Selector Guide

PART	ACCURACY GRADE	PIN-PACKAGE	PKG CODE	HEAT EXTRACTION
MAX9971ACCS*	A	80 TQFP-IDP†	—	Top
MAX9971BCCS*	B	80 TQFP-IDP†	—	Top
MAX9972ACCS*	A	80 TQFP-EP††	C80E-4	Bottom
MAX9972BCCS	B	80 TQFP-EP††	C80E-4	Bottom

**Future product—contact factory for availability.*

Note: *All devices are specified over the 0°C to +70°C operating temperature range.*

All versions available in both leaded and lead-free packaging. Specify lead-free by adding the "+" symbol at the end of the part number when ordering.

†*IDP = Inverted die pad.*

††*EP = Exposed paddle.*

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +9.4V
V_{SS} to GND .....-6.25V to +0.3V
V_{DD} to V_{SS} .....+15.7V
V_L to GND .....-0.3V to +5V
V_{DD} to GND .....-0.3V to +9.4V
DHV_, DTV_, DLV_, DATA_, RCV_, LDV_, DUT_ to GND .....V_{SS} to V_{DD}
CHV_, CLV_, CMPH_, CMPL_, COMPHI, COMPLO to GND .....V_{SS} to V_{DD}
FORCE_, SENSE_, PMU_ to GND .....V_{SS} to V_{DD}
$\overline{LD}$, DIN, SCLK, $\overline{CS}$ to GND .....-0.3V to +5V
DUT_, CMPH_, CMPL_ Short-Circuit Duration .....Continuous
DHV_, DLV_, DTV_ to Each Other .....V_{SS} to V_{DD}
CHV_, CLV_ to DUT_ .....V_{SS} to V_{DD}
DOUT to GND .....-0.3V to +5V
TEMP Short-Circuit Duration .....Continuous
Continuous Power Dissipation (T_A = +70°C)
80-Pin TQFP-EP (derate 35.7mW/°C above +70°C) 2857mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER (all specifications apply when DUT_ = DHV_, DUT_ = DTV_, or DUT_ = DLV_)							
DC CHARACTERISTICS							
Voltage Range				-2.2		+5.2	V
Gain		Measured at 0 and 3V	A grade	0.995	1	1.005	V/V
			B grade	0.95		1.05	
Gain Temperature Coefficient					50		ppm/°C
Offset		$V_{DHV\_}$ = 2V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1V	A grade			±7	mV
			B grade			±100	
Offset Temperature Coefficient					±250		µV/°C
Power-Supply Rejection Ratio	PSRR	V_{DD}, V_{SS} independently varied over full range				18	mV/V
Maximum DC Drive Current	$I_{DUT\_}$			±40		±90	mA
DC Output Resistance		$I_{DUT\_}$ = ±10mA (Note 2)		48.5	49.5	50.5	Ω
DC Output Resistance Variation		$I_{DUT\_}$ = -40mA to +40mA				2.5	Ω
DC Crosstalk		DHV to DLV and DTV: $V_{DLV\_}$ = $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -2.2V, +5.2V				5	mV
		DLV to DHV and DTV: $V_{DHV\_}$ = $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -2.2V, +5.2V				5	
		DTV to DHV and DLV: $V_{DHV\_}$ = $V_{DLV\_}$ = +1.5V, $V_{DTV\_}$ = -2.2V, +5.2V				5	
Linearity Error		0 to 3V (Note 3)				±5	mV
		Full range (Note 4)				±15	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (Note 5)						
Dynamic Output Current		(Note 1)	40			mA
Drive-Mode Overshoot, Undershoot, and Preshoot		200mV to 4V_{P-P} swing (Note 6)		5% +10		mV
Term-Mode Spike		$V_{DHV\_}$ = $V_{DTV\_}$ = 1V, $V_{DLV\_}$ = 0		25		mV
		$V_{DLV\_}$ = $V_{DTV\_}$ = 0, $V_{DHV\_}$ = 1V		25		
High-Impedance-Mode Spike		$V_{DLV\_}$ = -1.0V, $V_{DHV\_}$ = 0		25		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		25		
Prop Delay, Data to Output				2		ns
Prop-Delay Temperature Coefficient				10		ps/°C
Prop-Delay Match, t_{LH} vs. t_{HL}				30		ps
Prop-Delay Skew, Drivers Within Package				150		ps
Prop-Delay Change vs. Pulse Width		Relative to 12.5ns pulse, 3V_{P-P}, 40MHz, PW = 4ns to 21ns		20		ps
		Relative to 12.5ns pulse, 1V_{P-P}, 40MHz, PW = 2.5ns to 23.5ns		90		
Prop-Delay Change vs. Common-Mode Voltage		1V_{P-P}, $V_{DLV\_}$ = 0 to 3V, relative to delay at $V_{DLV\_}$ = 1V		80		ps
Prop Delay, Data to High Impedance		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V, both directions		1.8		ns
Prop Delay, Data to Term		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 0, both directions		1.6		ns
Minimum Voltage Swing		(Note 7)		25		mV
Rise/Fall Time		$V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0, 20% to 80%		0.7		ns
		$V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0, 20% to 80%		0.7		
		$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 10% to 90%	1.5	2.0	2.5	
		$V_{DHV\_}$ = 4V, $V_{DLV\_}$ = 0, R_L = 500Ω, 10% to 90%		2.6		
		$V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0, R_L = 500Ω, 10% to 90%		3.4		
Rise/Fall-Time Matching		$V_{DHV\_}$ = 1V to 5V		±5		%
Minimum Pulse Width (Note 8)		200mV, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0		1.8		ns
		1V, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0		2.4		
		3V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0		3.3		

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR (Note 9)							
DC CHARACTERISTICS (driver in high-impedance mode)							
Input Voltage Range				-2.2		+5.2	V
Differential Input Voltage		$V_{DUT\_}$ - $V_{CHV\_}$, $V_{DUT\_}$ - $V_{CLV\_}$		-7.4		+7.4	V
Hysteresis		$V_{CHV\_}$ = $V_{CLV\_}$ = 1.5V			8		mV
Input Offset Voltage		$V_{DUT\_}$ = 1.5V	A grade			±10	mV
			B grade			±100	
Input Offset Temperature Coefficient					25		µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = 0 and 3V		60			dB
Linearity Error (Note 10)		$V_{DUT\_}$ = 1.5V				±5	mV
		$V_{DUT\_}$ = -2.2V, +5.2V				±10	
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = 1.5V, supplies independently varied over full range				5	mV/V
AC CHARACTERISTICS (Note 11)							
Equivalent Input Bandwidth		Terminated (Note 12)			500		MHz
		High impedance (Note 13)			300		
Propagation Delay					3.9		ns
Prop-Delay Temperature Coefficient					4		ps/°C
Prop-Delay Match, t_{LH} to t_{HL}					120		ps
Prop-Delay Skew, Comparators Within Package		Same edges (LH and HL)			200		ps
Prop-Delay Dispersions vs. Common-Mode Voltage (Note 14)		0 to 4.9V			20		ps
		-1.9V to +4.9V			30		
Prop-Delay Dispersions vs. Overdrive		$V_{CHV\_}$ = $V_{CLV\_}$ = 0.1V to 0.9V, $V_{DUT\_}$ = $1V_{P-P}$, t_R = t_F = 500ps, 10% to 90% relative to timing at 50% point			220		ps
Prop-Delay Dispersions vs. Pulse Width		2ns to 23ns pulse width, relative to 12.5ns pulse width			±60		ps
Prop-Delay Dispersions vs. Slew Rate		0.5V/ns to 2V/ns			50		ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC OUTPUTS							
Reference Voltages COMPHI and COMPLO		(Note 15)		0		+3.6	V
Output High Voltage Offset		I_{OUT} = 0mA, relative to COMPHI at V_{COMPHI} = 1V				±50	mV
Output Low Voltage Offset		I_{OUT} = 0mA, relative to COMPLO at V_{COMPLO} = 0V				±50	mV
Output Resistance		$I_{CHV\_}$ = $I_{CLV\_}$ = ±10mA		40	50	60	Ω
Current Limit					25		mA
Rise/Fall Time		20% to 80%, $V_{CHV\_}$ = $1V_{P-P}$, load = T-line, 50Ω, > 1ns			0.7		ns
PASSIVE LOAD							
DC CHARACTERISTICS ($R_{DUT\_}$ ≥ 10MΩ)							
LDV_ Voltage Range				-2.2		+5.2	V
Gain				0.99		1.01	V/V
Gain Temperature Coefficient					0.02		%/°C
Offset						±100	mV
Offset Temperature Coefficient					0.02		mV/°C
Power-Supply Rejection Ratio	PSRR				10		mV/V
Output Resistance Tolerance—High Value		$I_{DUT\_}$ = ±0.2mA, $V_{LDV\_}$ = 1.5V	A grade	7.125	7.5	7.875	kΩ
			B grade	4.200	6.0	7.875	
Output Resistance Tolerance—Low Value		$I_{DUT\_}$ = ±0.1mA, $V_{LDV\_}$ = 1.5V	A grade	1.90	2.0	2.10	kΩ
			B grade	1.05	1.5	2.10	
Switch Resistance Variation		Relative to 1.5V	0 to 3V		±10		%
			Full range		±30		
Maximum Output Current (Note 16)		$V_{LDV\_}$ = -2V, $V_{DUT\_}$ = +5V			±4		mA
		$V_{LDV\_}$ = +5V, $V_{DUT\_}$ = -2V			±4		
Linearity Error, Full Range		Measured at -2.2V, +1.5V, and +5.2V (Note 16)				±25	mV
AC CHARACTERISTICS							
Settling Time, LDV_ to Output		$V_{LDV\_}$ = -2V to +5V step, $R_{DUT\_}$ = 100kΩ (Note 17)			0.5		µs
Output Transient Response		$V_{LDV\_}$ = +1.5V, $V_{DUT\_}$ = -2V to +5V square wave at 1MHz, $R_{DUT\_}$ = 50Ω			20		ns

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMU SWITCHES (FORCE_, SENSE_, PMU_)						
Voltage Range			-2.2		+5.2	V
Force Switch Resistance		$V_{FORCE\_}$ = 1.5V, $I_{PMU\_}$ = ±10mA			40	Ω
Force Switch Compliance		$V_{PMU\_}$ = 6.2V, $V_{FORCE\_}$ set to make $I_{FORCE\_}$ = 30mA	25			mA
		$V_{PMU\_}$ = -3.2V, $V_{FORCE\_}$ set to make $I_{FORCE\_}$ = -30mA	25			
Force Switch Resistance Variation (Note 18)		0 to 3V		±10		%
		Full range		±30		
Sense Switch Resistance			700	1000	1300	Ω
Sense Switch Resistance Variation		Relative to 1.3V, full range		±30		%
PMU_ Capacitance		Force-and-sense switches open		5		pF
FORCE_ Capacitance				5		pF
SENSE_ Capacitance				0.2		pF
FORCE_ External Capacitance		Allowable external capacitance		2		nF
SENSE_ External Capacitance		Allowable external capacitance		1		nF
FORCE_ and SENSE_ Switching Speed		Connect or disconnect		10		µs
PMU_ Leakage		FORCE EN_ = SENSE EN_ = 0, $V_{FORCE\_}$ = $V_{SENSE\_}$ = -2.2V to +5.2V		±0.5	±5	nA
TOTAL FUNCTION						
DUT_						
Leakage, High-Impedance Mode		Load switches open, $V_{DUT\_}$ = +5.2V, $V_{CLV\_}$ = $V_{CHV\_}$ = -2.2V, $V_{DUT\_}$ = -2.2V, $V_{CLV\_}$ = $V_{CHV\_}$ = +5.2V, full range			2	µA
Leakage, Low-Leakage Mode		Full range		±1	±20	nA
Low-Leakage Recovery Time		(Note 19)		10		µs
Combined Capacitance		Term mode		2		pF
		High-impedance mode		5		
Load Resistance		(Note 20)		1		GΩ
Load Capacitance		(Note 20)		12		nF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE INPUTS (DHV_, DTV_, DLV_, DATA_, RCV_, CHV_, CLV_, LDV_, COMPHI, COMPLO)						
Input Bias Current					±100	µA
Input Bias Current Temperature Coefficient				±200		nA/°C
Settling to Output		0.1% of full-scale step		10		µs
DIGITAL INPUTS (DATA_, RCV_, $\overline{LD}$, DIN, SCLK, $\overline{CS}$)						
Input High Voltage		(Note 21)	V_L / 2 + 0.2		+3.6	V
Input Low Voltage		(Note 21)	-0.3		V_L / 2 - 0.2	V
Input Bias Current					100	µA
SERIAL DATA OUTPUT (DOUT)						
Output High Voltage		I_{OH} = -1mA	V_L - 0.4		V_L	V
Output Low Voltage		I_{OL} = 1mA	0		+0.4	V
Output Rise and Fall Time		C_L = 10pF		1.1		ns
SCLK to DOUT Delay		C_L = 10pF	t_{DH}		t_{SCLK} - t_{DS} - 2ns	ns
SERIAL-INTERFACE TIMING (Note 22)						
SCLK Frequency					50	MHz
SCLK Pulse-Width High	t_{CH}		10			ns
SCLK Pulse-Width Low	t_{CL}		10			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}		0			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		15			ns
DIN to SCLK High Setup	t_{DS}		3.5			ns
DIN to SCLK High Hold	t_{DH}		1			ns
$\overline{CS}$ High to $\overline{LOAD}$ Low Setup	t_{CLL}		6			ns
$\overline{LD}$ Low Hold Time	t_{LDW}		5			ns
$\overline{LD}$ High to Any Activity			0			ns
V_L Rising to $\overline{CS}$ Low		Power-on delay		2		µs
TEMP SENSOR						
Nominal Voltage		T_J = +27°C		3.00		V
Temperature Coefficient				+10		mV/°C
Output Resistance				500		Ω

Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{COMPHI} = +1V, V_{COMPLO} = 0, $V_{LDV\_}$ = 0, LOAD EN LOW = LOAD EN HIGH = 0, T_J = +75°C. All temperature coefficients measured at T_J = +50°C to +100°C, unless otherwise noted.) (Note 1)

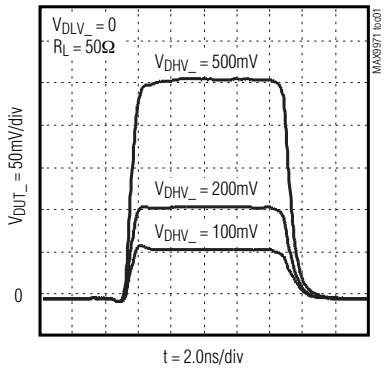
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	(Note 23)	7.6	8	8.4	V
Negative Supply Voltage	V_{SS}	(Note 23)	-5.25	-5	-4.75	V
Logic Supply Voltage	V_L		2.3		3.6	V
Positive Supply Current	I_{DD}	f_{OUT} = 0MHz		97	120	mA
Negative Supply Current	I_{SS}	f_{OUT} = 0MHz		99	120	mA
Logic Supply Current	I_L			0.15	0.30	mA
Static Power Dissipation		f_{OUT} = 0MHz		1.3	1.5	W
Operating Power Dissipation		f_{OUT} = 100Mbps (Note 24)		1.4		W

Note 1: All minimum and maximum specifications are 100% production tested except driver dynamic output current, which is guaranteed by design. All specifications are with DUT_ and PMU_ electrically isolated, unless otherwise noted.
Note 2: Nominal target value is 49.5Ω. Contact factory for alternate trim selections within the 45Ω to 55Ω range.
Note 3: Measured at 1.5V, relative to a straight line through 0 and 3V.
Note 4: Measured at end points, relative to a straight line through 0 and 3V.
Note 5: DUT_ is terminated with 50Ω to ground, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, unless otherwise specified. DATA_ and RCV_ logic levels are V_{HIGH} = 2V, V_{LOW} = 1V.
Note 6: Undershoot is any reflection of the signal back towards its starting voltage after it has reached 90% of its swing. Preshoot is any aberration in the signal before it reaches 10% of its swing.
Note 7: At the minimum voltage swing, undershoot is less than 20%. DHV_ and DLV_ references are adjusted to result in the specified swing.
Note 8: At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.
Note 9: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.
Note 10: Relative to a straight line through 0 and 3V.
Note 11: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to 1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V, t_R = t_F = 500ps, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = +0.5V. Comparator outputs are terminated with 50Ω to GND. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to midpoint of nominal comparator output swing.
Note 12: Terminated is defined as driver in drive mode and set to zero volts.
Note 13: High impedance is defined as driver in high-impedance mode.
Note 14: $V_{DUT\_}$ = 200mV_{P-P}. Propagation delay is compared to a reference time at 1.5V.
Note 15: The comparator meets all its timing specifications with the specified output conditions when the output current is less than 15mA, V_{COMPHI} > V_{COMPLO}, and V_{COMPHI} - V_{COMPLO} ≤ 1V. Higher voltage swings are valid but AC performance may degrade.
Note 16: LOAD EN LOW = LOAD EN HIGH = 1.
Note 17: Waveform settles to within 5% of final value into load 100kΩ.
Note 18: $I_{PMU\_}$ = ±2mA at $V_{FORCE\_}$ = -2.2V, +1.5V, and +5.2V. Percent variation relative to value calculated at $V_{FORCE\_}$ = +1.5V.
Note 19: Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_.
Note 20: Load at end of 2ns transmission line; for stability only, AC performance may be degraded.
Note 21: The driver meets all of its timing specifications over the specified digital input voltage range.
Note 22: Timing characteristics with V_{LOGIC} = 3V.
Note 23: Specifications are simulated and characterized over the full power-supply range. Production tests are performed with power supplies at typical values.
Note 24: All channels driven at 3V_{P-P}, load = 2ns, 50Ω transmission line terminated with 3pF.

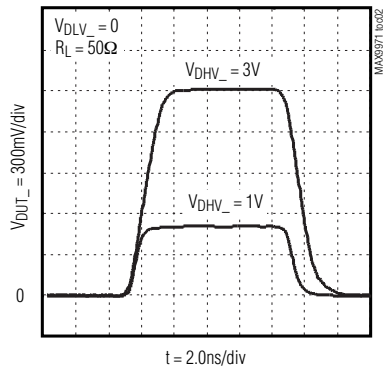
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

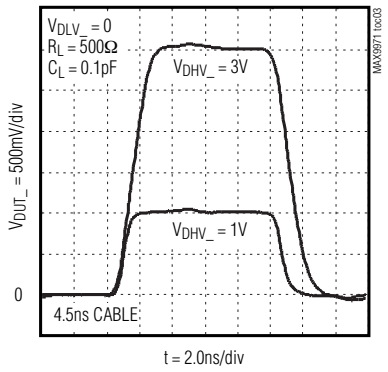
DRIVER SMALL-SIGNAL RESPONSE



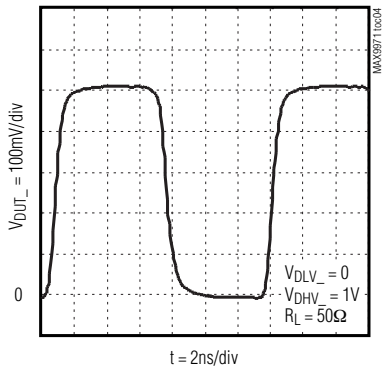
DRIVER LARGE-SIGNAL RESPONSE



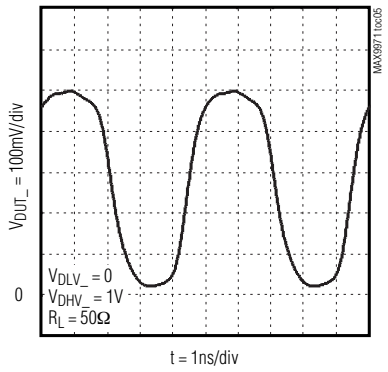
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



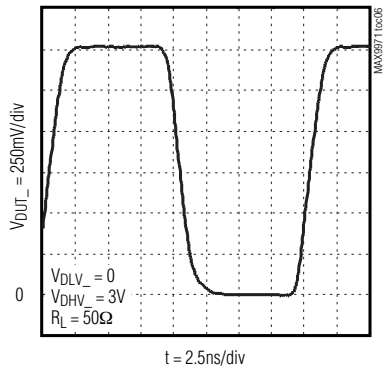
DRIVER 1VP-P, 150Mbps SIGNAL RESPONSE



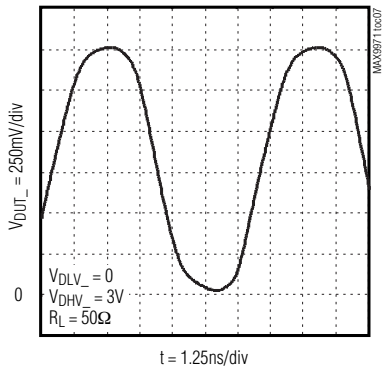
DRIVER 1VP-P, 400Mbps SIGNAL RESPONSE



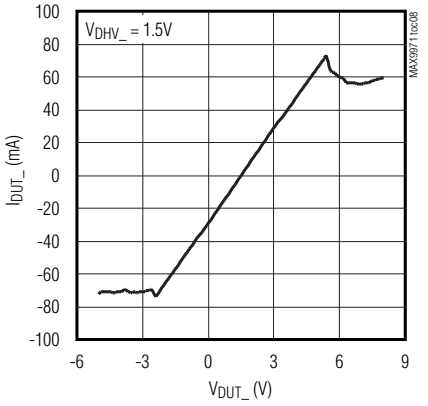
DRIVER 3VP-P, 100Mbps SIGNAL RESPONSE



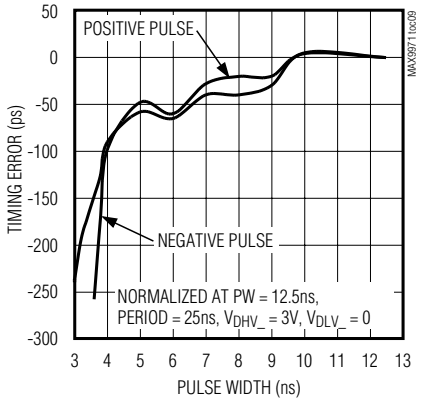
DRIVER 3VP-P, 250Mbps SIGNAL RESPONSE



DRIVER DC CURRENT-LIMIT AND OVERVOLTAGE RESPONSE



DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH

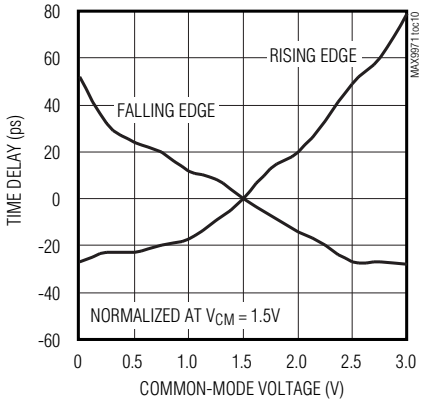


Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

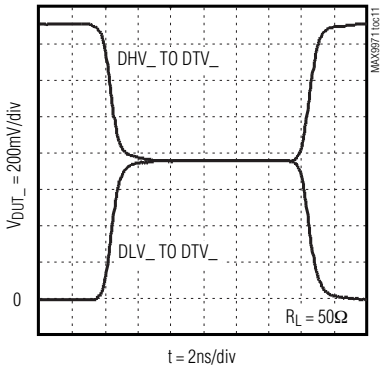
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

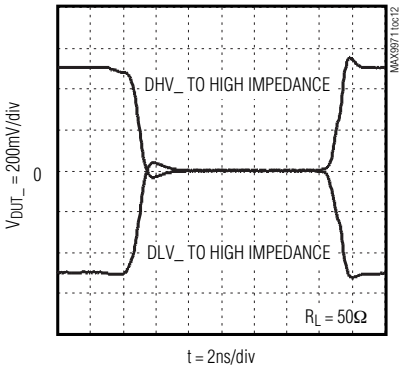
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



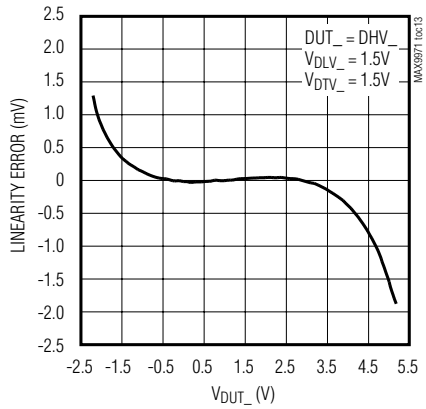
DRIVE-TO-TERM TRANSITION



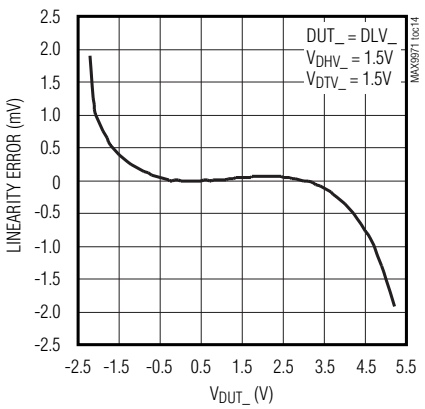
DRIVE-TO-HIGH-IMPEDANCE TRANSITION



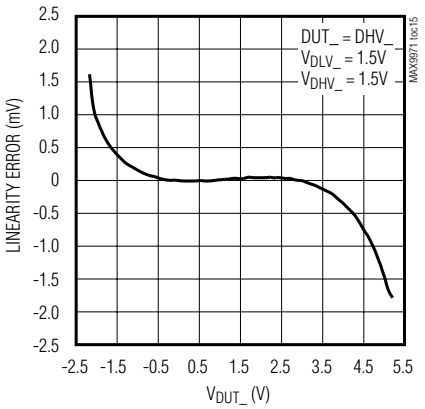
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



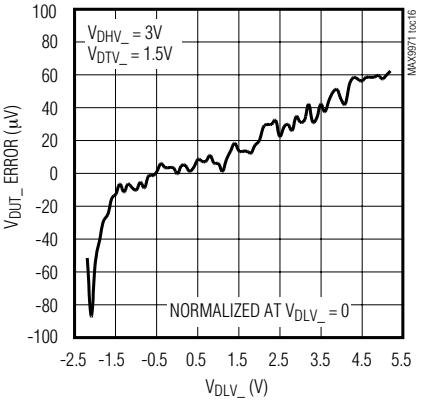
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



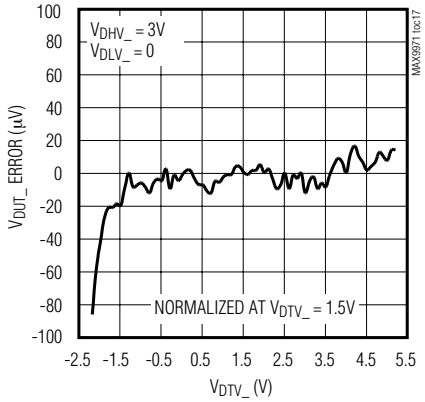
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



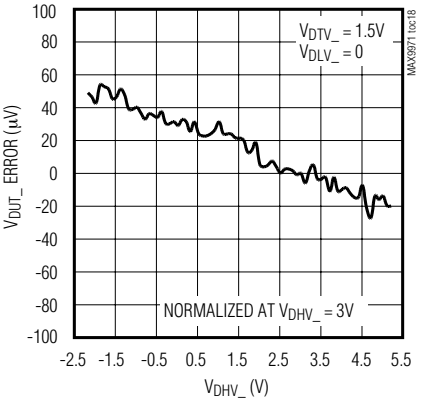
CROSSTALK, DUT_ DRIVEN BY DHV_ WITH DLV_ VARIED



CROSSTALK, DUT_ DRIVEN BY DHV_ WITH DTV_ VARIED



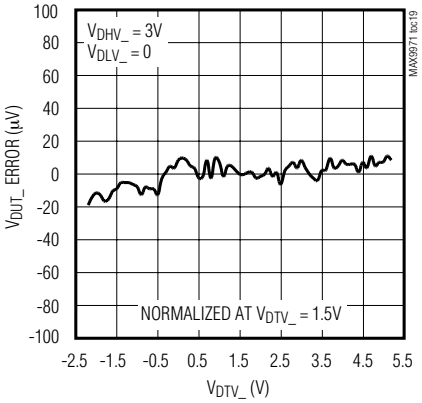
CROSSTALK, DUT_ DRIVEN BY DLV_ WITH DHV_ VARIED



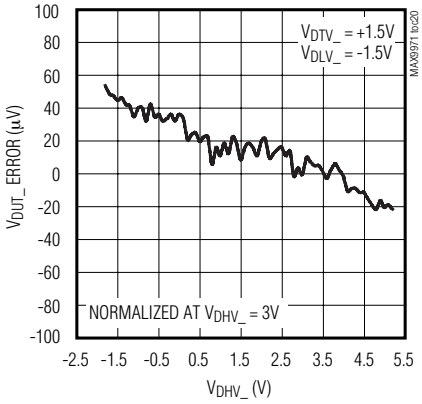
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

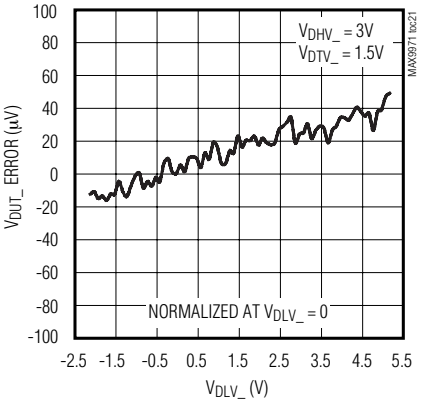
CROSSTALK, DUT_ DRIVEN BY DLV_ WITH DTV_ VARIED



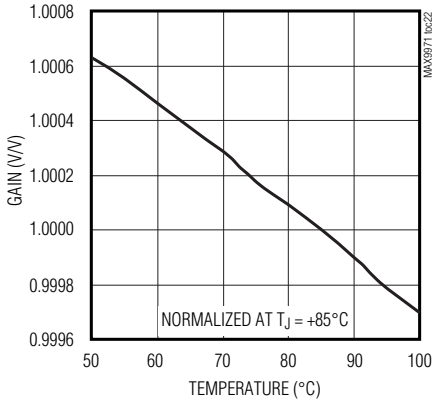
CROSSTALK, DUT_ DRIVEN BY DTV_ WITH DHV_ VARIED



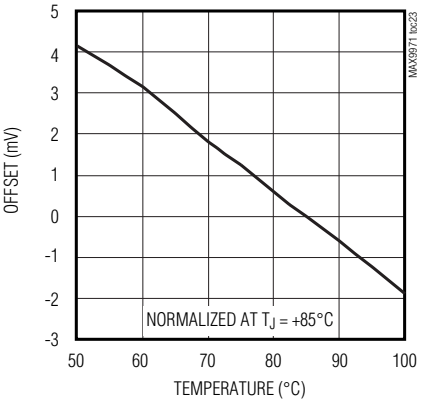
CROSSTALK, DUT_ DRIVEN BY DTV_ WITH DLV_ VARIED



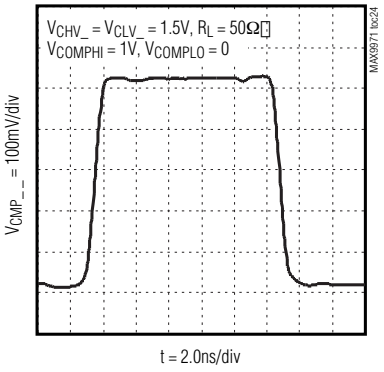
DRIVER GAIN vs. TEMPERATURE



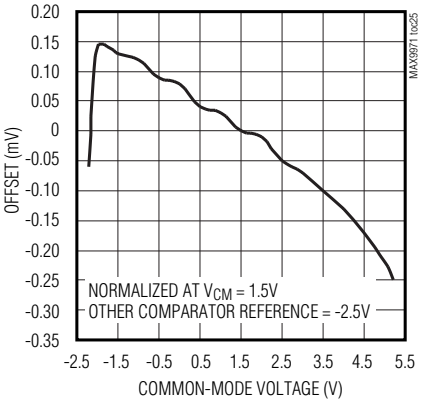
DRIVER OFFSET vs. TEMPERATURE



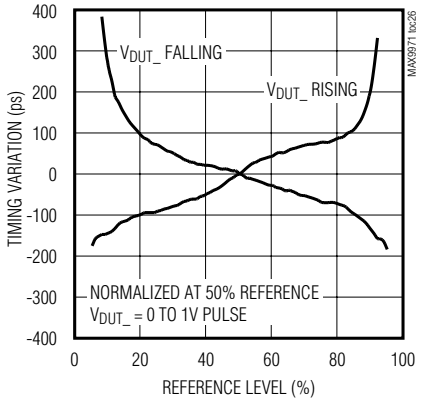
COMPARATOR RESPONSE TO 0 TO 3V SIGNAL



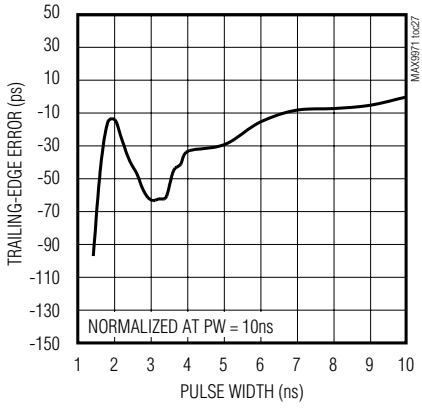
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



COMPARATOR WAVEFORM TRACKING



COMPARATOR TIMING VARIATION vs. PULSE WIDTH

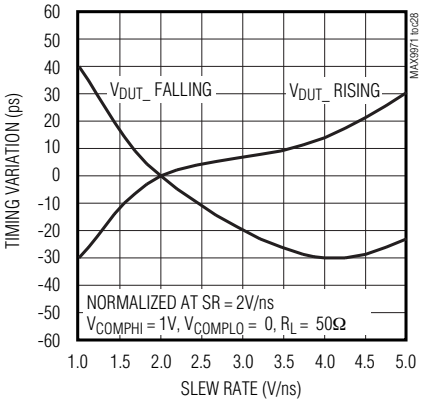


Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

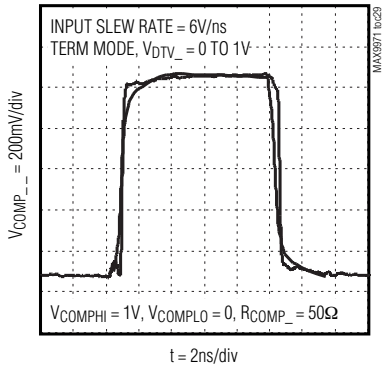
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

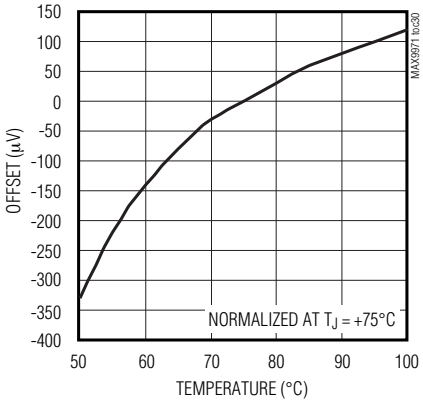
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE



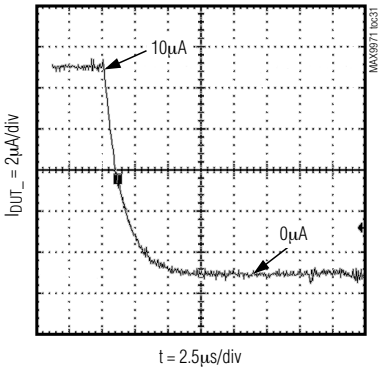
COMPARATOR RESPONSE vs. HIGH SLEW-RATE OVERDRIVE



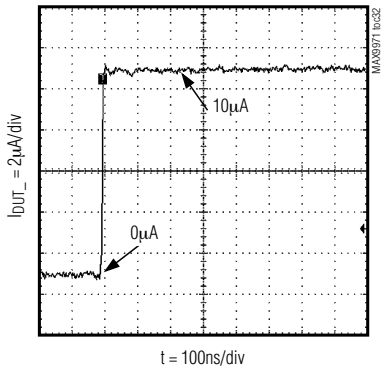
COMPARATOR OFFSET vs. TEMPERATURE



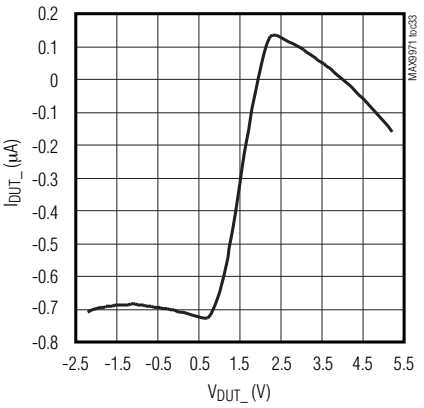
DRIVE 1V TO LOW-LEAKAGE TRANSITION



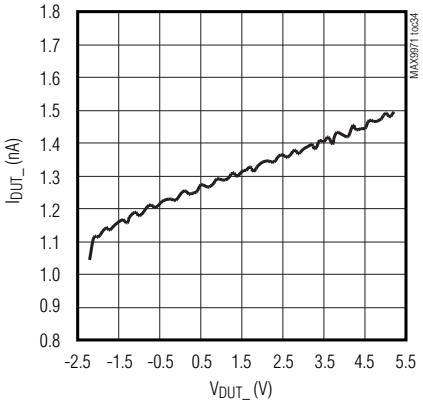
LOW LEAKAGE TO DRIVE 1V TRANSITION



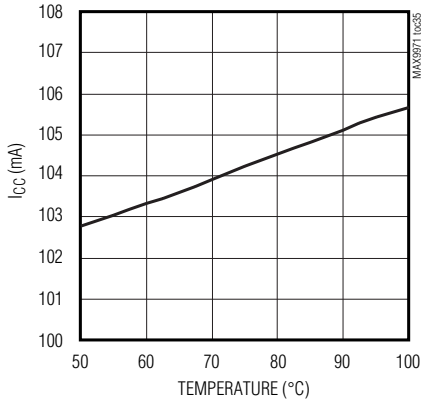
HIGH-IMPEDANCE LEAKAGE AT DUT_ vs. DUT_ VOLTAGE



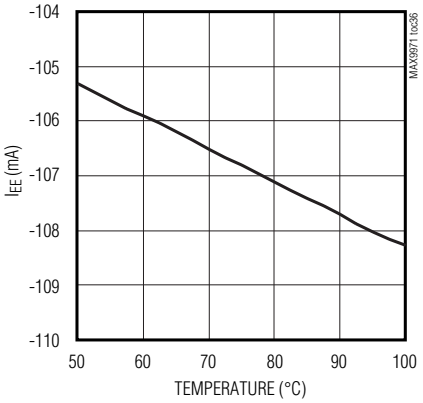
LOW-LEAKAGE CURRENT vs. DUT_VOLTAGE



ICC SUPPLY CURRENT vs.TEMPERATURE



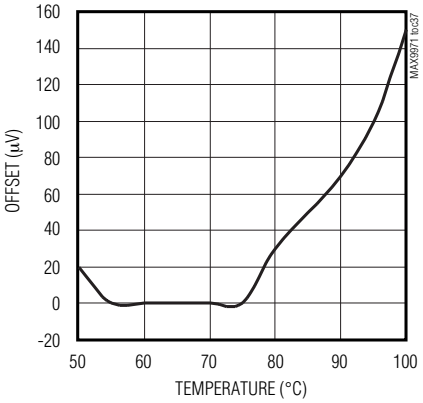
IEE SUPPLY CURRENT vs.TEMPERATURE



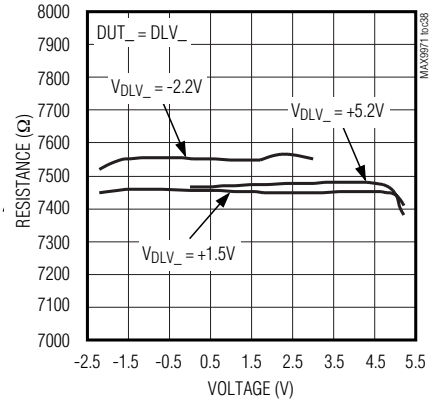
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

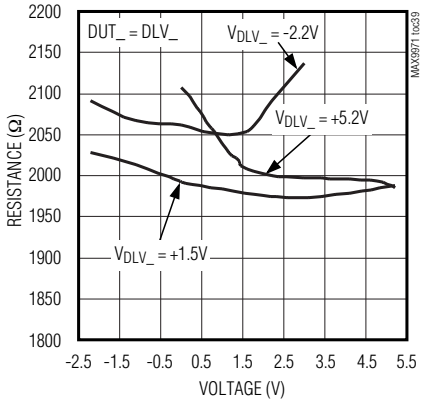
PASSIVE LOAD OFFSET vs. TEMPERATURE



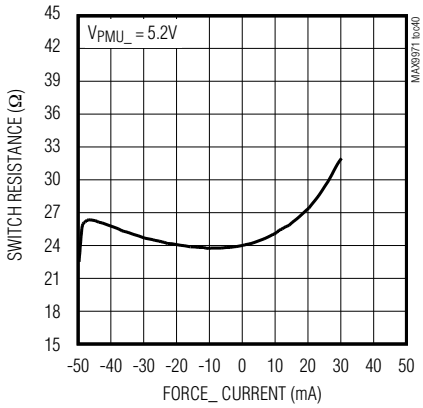
PASSIVE LOAD HIGH RESISTOR vs. VOLTAGE



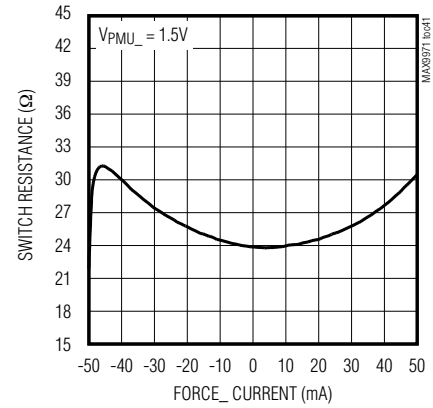
PASSIVE LOAD LOW RESISTOR vs. VOLTAGE



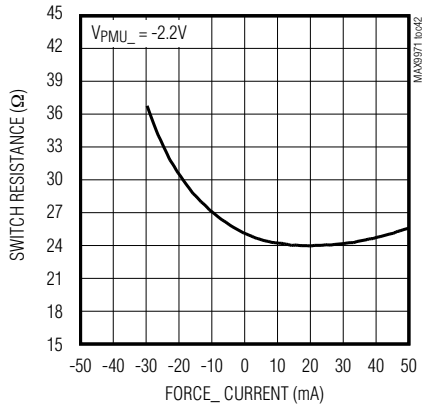
PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



PMU_ FORCE_ SWITCH RESISTANCE vs. FORCE_ CURRENT



Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

Pin Description

PIN		NAME	FUNCTION
MAX9972	MAX9971		
1	60	DATA1	Channel 1 Multiplexer Control Input. Selects driver 1 input from DHV1 or DLV1 in drive mode. See Table 1 and Figure 2.
2	59	RCV1	Channel 1 Multiplexer Control Input. Sets channel 1 mode to drive or receive. See Table 1 and Figure 2.
3, 8, 13, 18, 51	10, 43, 48, 53, 58	GND	Analog Ground
4	57	CMPH1	Channel 1 High-Side Comparator Output
5	56	CMPL1	Channel 1 Low-Side Comparator Output
6	55	DATA2	Channel 2 Multiplexer Control Input. Selects driver 2 input from DHV2 or DLV2 in drive mode. See Table 1 and Figure 2.
7	54	RCV2	Channel 2 Multiplexer Control Input. Sets channel 2 mode to drive or receive. See Table 1 and Figure 2.
9	52	CMPH2	Channel 2 High-Side Comparator Output
10	51	CMPL2	Channel 2 Low-Side Comparator Output
11	50	CMPL3	Channel 3 Low-Side Comparator Output
12	49	CMPH3	Channel 3 High-Side Comparator Output
14	47	RCV3	Channel 3 Multiplexer Control Input. Sets channel 3 mode to drive or receive. See Table 1 and Figure 2.
15	46	DATA3	Channel 3 Multiplexer Control Input. Selects driver 3 input from DHV3 or DLV3 in drive mode. See Table 1 and Figure 2.
16	45	CMPL4	Channel 4 Low-Side Comparator Output
17	44	CMPH4	Channel 4 High-Side Comparator Output
19	42	RCV4	Channel 4 Multiplexer Control Input. Sets channel 4 mode to drive or receive. See Table 1 and Figure 2.
20	41	DATA4	Channel 4 Multiplexer Control Input. Selects driver 4 input from DHV4 or DLV4 in drive mode. See Table 1 and Figure 2.
21	40	DHV4	Channel 4 Driver High Voltage Input
22	39	DLV4	Channel 4 Driver Low Voltage Input
23	38	DTV4	Channel 4 Driver Termination Voltage Input
24	37	CHV4	Channel 4 Threshold Voltage Input for High-Side Comparator
25	36	CLV4	Channel 4 Threshold Voltage Input for Low-Side Comparator
26	35	DHV3	Channel 3 Driver High Voltage Input
27	34	DLV3	Channel 3 Driver Low Voltage Input
28	33	DTV3	Channel 3 Driver Termination Voltage Input
29	32	CHV3	Channel 3 Threshold Voltage Input for High-Side Comparator
30	31	CLV3	Channel 3 Threshold Voltage Input for Low-Side Comparator
31	30	DGND	Digital Ground Connection
32	29	DOUT	Serial-Interface Data Output
33	28	$\overline{LD}$	Load Input. Latches data from the serial input register to the control register on rising edge. Transparent when low.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9972	MAX9971		
34	27	DIN	Serial-Interface Data Input
35	26	SCLK	Serial Clock
36	25	$\overline{CS}$	Chip Select
37	24	SENSE4	Channel 4 PMU Sense Connection
38	23	FORCE4	Channel 4 PMU Force Connection
39	22	SENSE3	Channel 3 PMU Sense Connection
40	21	FORCE3	Channel 3 PMU Force Connection
41	20	TEMP	Temperature Sensor Output
42, 47, 52, 56, 60	1, 5, 9, 14, 19	V_{DD}	Positive Power-Supply Input
43	18	DUT4	Channel 4 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 4.
44	17	PMU4	Channel 4 Parametric Measurement Connection. PMU switch I/O node for channel 4.
45, 50, 53, 57	4, 8, 11, 16	V_{SS}	Negative Power-Supply Input
46	15	V_L	Logic Power-Supply Input
48	13	DUT3	Channel 3 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 3.
49	12	PMU3	Channel 3 Parametric Measurement Connection. PMU switch I/O node for channel 3.
54	7	PMU2	Channel 2 Parametric Measurement Connection. PMU switch I/O node for channel 2.
55	6	DUT2	Channel 2 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 2.
58	3	PMU1	Channel 1 Parametric Measurement Connection. PMU switch I/O node for channel 1.
59	2	DUT1	Channel 1 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 1.
61	80	FORCE2	Channel 2 PMU Force Connection
62	79	SENSE2	Channel 2 PMU Sense Connection
63	78	FORCE1	Channel 1 PMU Force Connection
64	77	SENSE1	Channel 1 PMU Sense Connection
65	76	COMPLO	Comparator Output-Low Voltage Reference Input
66	75	COMPHI	Comparator Output-High Voltage Reference Input
67	74	LDV4	Channel 4 Load Voltage Input
68	73	LDV3	Channel 3 Load Voltage Input
69	72	LDV2	Channel 2 Load Voltage Input
70	71	LDV1	Channel 1 Load Voltage Input
71	70	CLV2	Channel 2 Threshold Voltage Input for Low-Side Comparator
72	69	CHV2	Channel 2 Threshold Voltage Input for High-Side Comparator
73	68	DTV2	Channel 2 Driver Termination Voltage Input
74	67	DLV2	Channel 2 Driver Low Voltage Input
75	66	DHV2	Channel 2 Driver High Voltage Input
76	65	CLV1	Channel 1 Threshold Voltage Input for Low-Side Comparator
77	64	CHV1	Channel 1 Threshold Voltage Input for High-Side Comparator
78	63	DTV1	Channel 1 Driver Termination Voltage Input
79	62	DLV1	Channel 1 Driver Low Voltage Input
80	61	DHV1	Channel 1 Driver High Voltage Input
—	—	EP	Exposed Pad. Leave unconnected or connect to V_{SS}.

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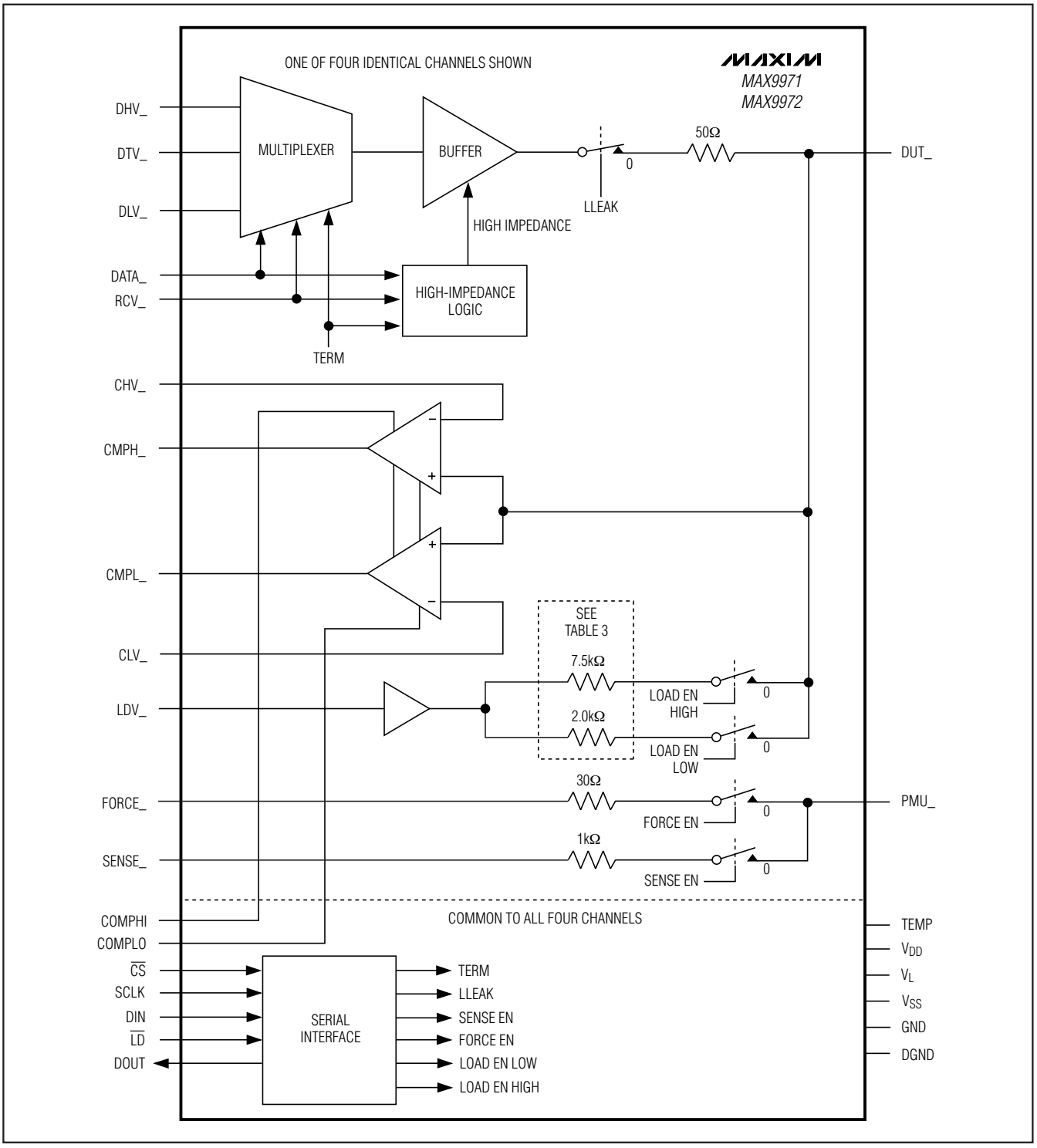

Figure 1. Block Diagram

Detailed Description

The MAX9971/MAX9972 are four-channel, pin-electronics ICs for automated test equipment that include, for each channel, a three-level pin driver, a window comparator, a passive load, and a Kelvin instrument connection (Figure 1). All functions feature a -2.2V to +5.2V operating range and the drivers include both high-impedance and active-termination (3rd-level drive) modes. The comparators feature programmable output voltages, allowing optimization for different CMOS interface standards. The loads have selectable output resistance for optimizing DUT current loading. The Kelvin paths allow accurate connection of an instrument with ±25mA source/sink capability. Additionally, the MAX9971/MAX9972 offer a low-leakage mode that reduces DUT_ leakage current to less than 20nA.

The MAX9971/MAX9972 are available in two grades. The A-grade devices provide tighter tolerances for driver gains and offsets, comparator offsets, and load resistor values. This allows reference levels to be shared across multiple channels in cost-sensitive systems. The B-grade devices are intended for system designs that incorporate independent reference levels for each channel.

Each of the four channels feature single-ended CMOS-compatible inputs, DATA_ and RCV_, for control of the driver signal path (Figure 2). The MAX9971/MAX9972 modal operation is programmed through a 3-wire, low-voltage CMOS-compatible serial interface.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs; DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_, and mode-control bit TERM (Table 1). DATA_ and RCV_ are single-ended inputs with threshold levels equal to V_L / 2. Each channel's threshold levels are independently generated to minimize crosstalk.

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). High-speed input RCV_ and mode-control bits TERM and LLEAK control these modes. In high-impedance mode, the bias current at DUT_ is less than 2µA over the -2.2V to +5.2V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 20nA, and signal tracking slows.

The nominal driver output resistance is 50Ω. Custom resistance values from 45Ω to 51Ω are possible; consult factory for further information.

Table 1. Driver Channel Control Signals

EXTERNAL CONNECTIONS		INTERNAL CONTROL BITS		DRIVER OUTPUT	DRIVER MODE
RCV_	DATA_	TERM	LLEAK		
0	0	X	0	DUT_ = DLV_	Drive
0	1	X	0	DUT_ = DHV_	Drive
1	X	0	0	High Impedance	Receive
1	X	1	0	DUT_ = DTV_	Receive
X	X	X	1	Low Leak	Low Leakage

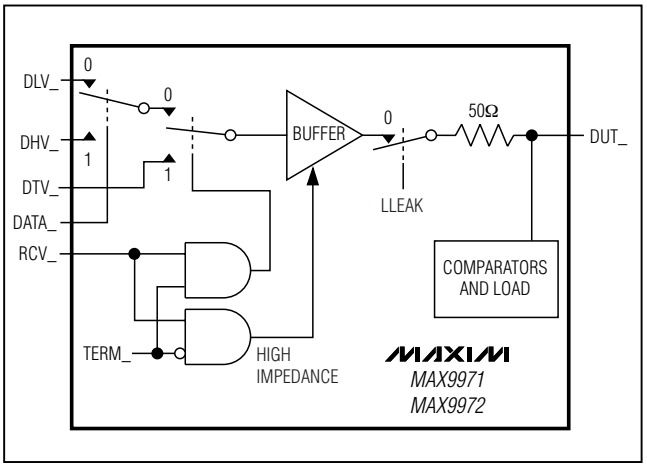

Figure 2. Multiplexer and Driver Channel

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Comparators

The MAX9971/MAX9972 provide two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (see Figure 1). Comparator outputs are a logical result of the input conditions, as indicated in Table 2.

The comparator output voltages are easily interfaced to a wide variety of logic standards. Use buffered inputs COMPHI and COMPLO to set the high and low output voltages. For correct operation, COMPHI should be greater than or equal to COMPLO. The comparator 50Ω output impedance provides source termination (Figure 3).

Passive Load

The MAX9971/MAX9972 channels each feature a passive load consisting of a buffered input voltage, LDV_, connected to DUT_ through two resistive paths (Figure 1). Each path connects to DUT_ individually by a switch controlled through the serial interface. Programming options include none (load disconnected), either, or both paths connected. The resistor values vary depending on the accuracy grade of the device, as shown in Table 3. The loads facilitate fast open/short testing in conjunction with the comparator, and pullup of open-drain DUT_ outputs.

Parametric Switches

Each of the four MAX9971/MAX9972 channels provides force-and-sense paths for connection of a PMU or other DC resource to the device-under-test (Figure 1). Each force-and-sense switch is independently controlled though the serial interface providing maximum application flexibility. PMU_ and DUT_ are provided on separate pins allowing designs that do not require the parametric switch feature to avoid the added capacitance of PMU_. It also allows PMU_ to connect to DUT_ either directly or with an impedance-matching network.

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port places the MAX9971/MAX9972 into a very-low-leakage state (see the *Electrical Characteristics* table). This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK control is independent for each channel.

When DUT_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Table 2. Comparator Logic

DUT_ > CHV_	DUT_ > CLV_	CMPH_	CMPL_
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

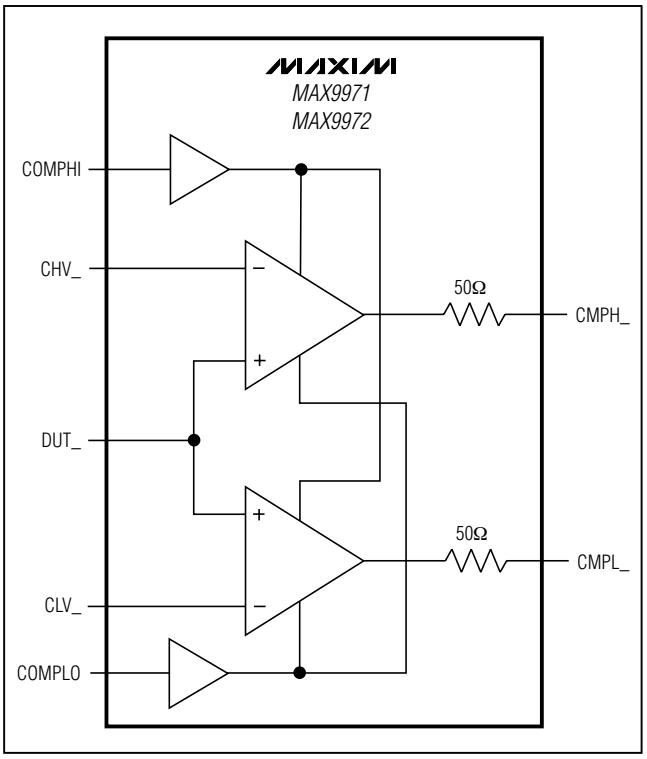


Figure 3. Complementary 50Ω Comparator Outputs

Table 3. Passive Load Resistance Values

ACCURACY GRADE	HIGH RESISTOR (kΩ)	LOW RESISTER (kΩ)
A	7.5	2
B	6	1.5

Temperature Monitor

Each device supplies a single temperature output signal, TEMP, that asserts a nominal 3.43V output voltage at a +70°C (343K) die temperature. The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 500Ω, typical.

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9971/MAX9972 modes (Figure 4). Control data flow into a 12-bit shift register (MSB first) and are latched when $\overline{CS}$ is taken high. Data from the shift register are then loaded to the per-channel control latches as determined by bits D8–D11, and indicated in Figure 4 and Table 4. The latches contain the six mode bits for each channel of the device. The mode bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel. Transfer data asynchronously from the input registers to the channel registers by forcing $\overline{LD}$ low. With $\overline{LD}$ always low, data transfer on the rising edge of $\overline{CS}$.

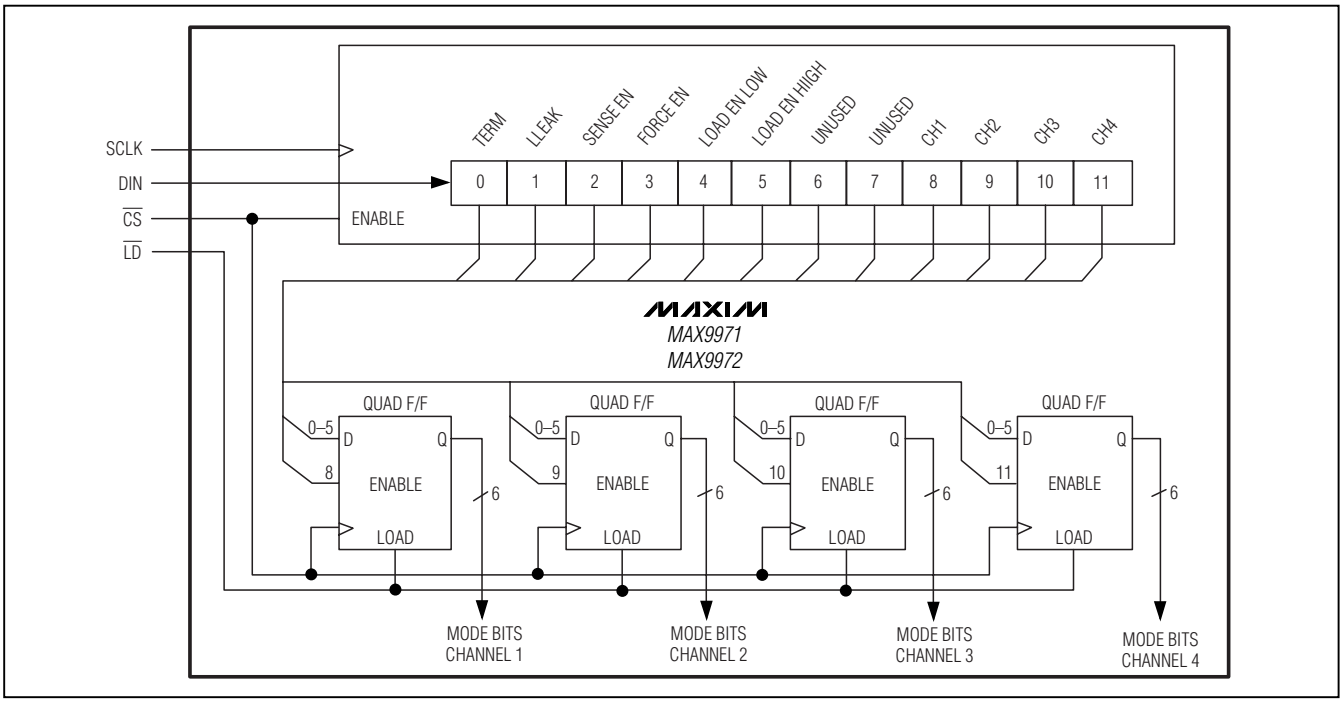


Figure 4. Serial Interface

Table 4. Control Register Bit Functions

BIT	NAME	FUNCTION	BIT STATE		POWER-UP STATE
			0	1	
0	TERM	Term Mode Control	High Impedance	Term Mode	0
1	LLEAK	Assert Low-Leakage Mode	Term Mode	Low Leakage	0
2	SENSE EN	Enable Sense Switch	Disabled	Enabled	0
3	FORCE EN	Enable Force Switch	Disabled	Enabled	0
4	LOAD EN LOW	Enable Low Load Resistor	Disabled	Enabled	0
5	LOAD EN HIGH	Enable High Load Resistor	Disabled	Enabled	0
6	—	Unused	X	X	0
7	—	Unused	X	X	0
8	CH1	Update Channel 1 Control Register	Disabled	Enabled	1
9	CH2	Update Channel 2 Control Register	Disabled	Enabled	1
10	CH3	Update Channel 3 Control Register	Disabled	Enabled	1
11	CH4	Update Channel 4 Control Register	Disabled	Enabled	1

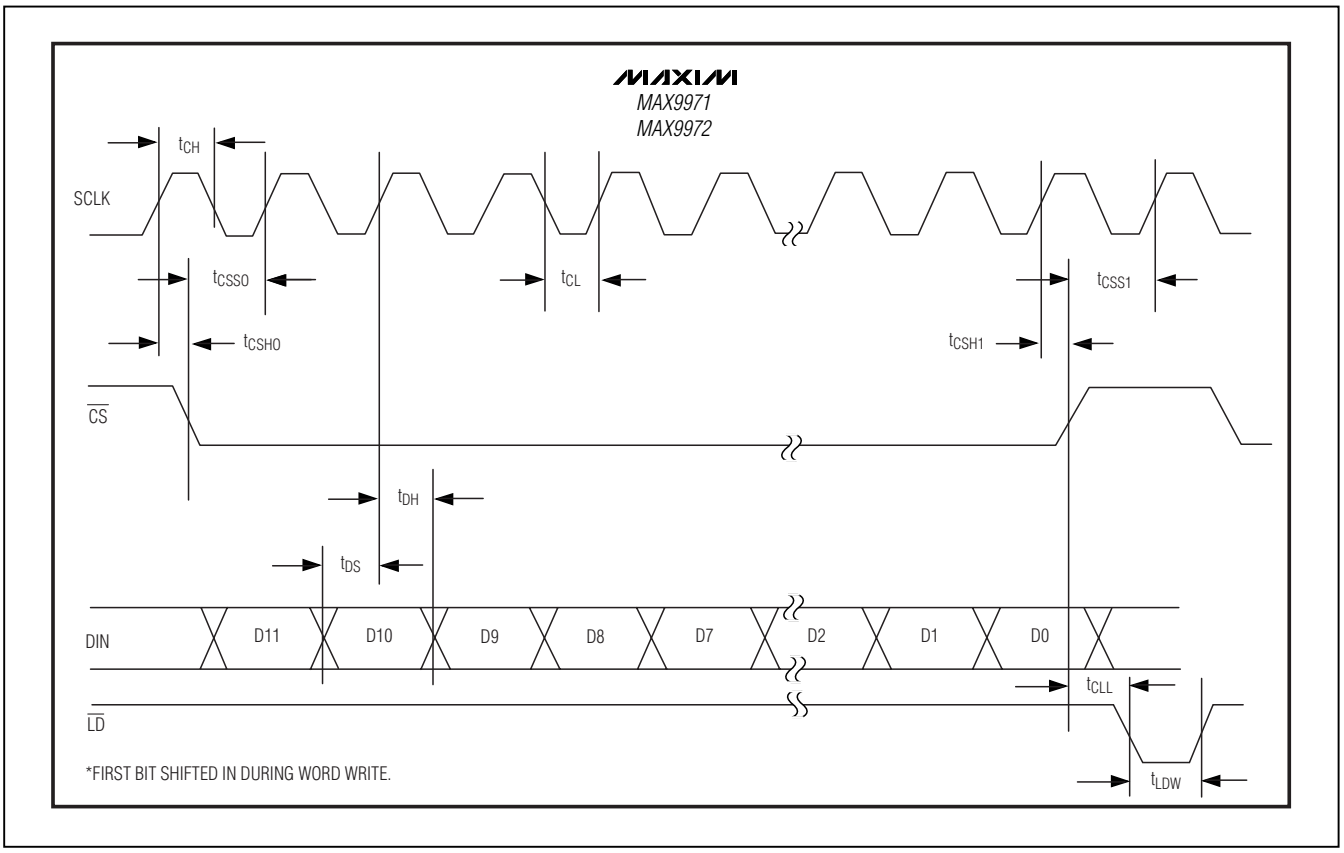


Figure 5. Serial-Interface Timing

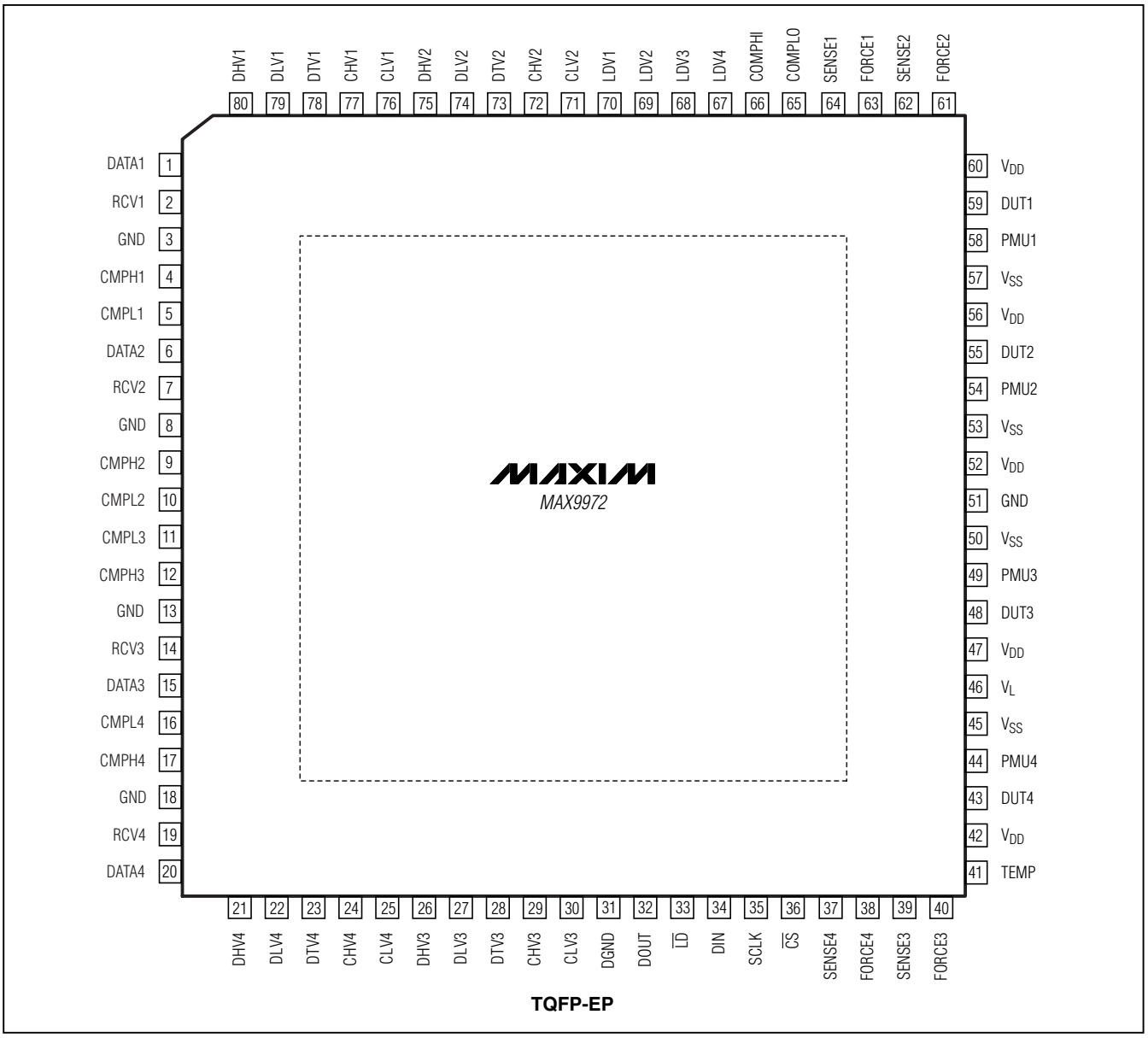
Heat Removal

With adequate airflow, no external heat sinking is needed under most operating conditions. If excess heat must be dissipated through the exposed paddle, solder it to circuit board copper (MAX9972) or use an external heat sink (MAX9971). The exposed paddle must be either left unconnected, isolated, or connected to V_{SS}.

Power Minimization

To minimize power consumption, activate only the needed channels. Each channel placed in low-leakage mode saves approximately 240mW.

Pin Configurations



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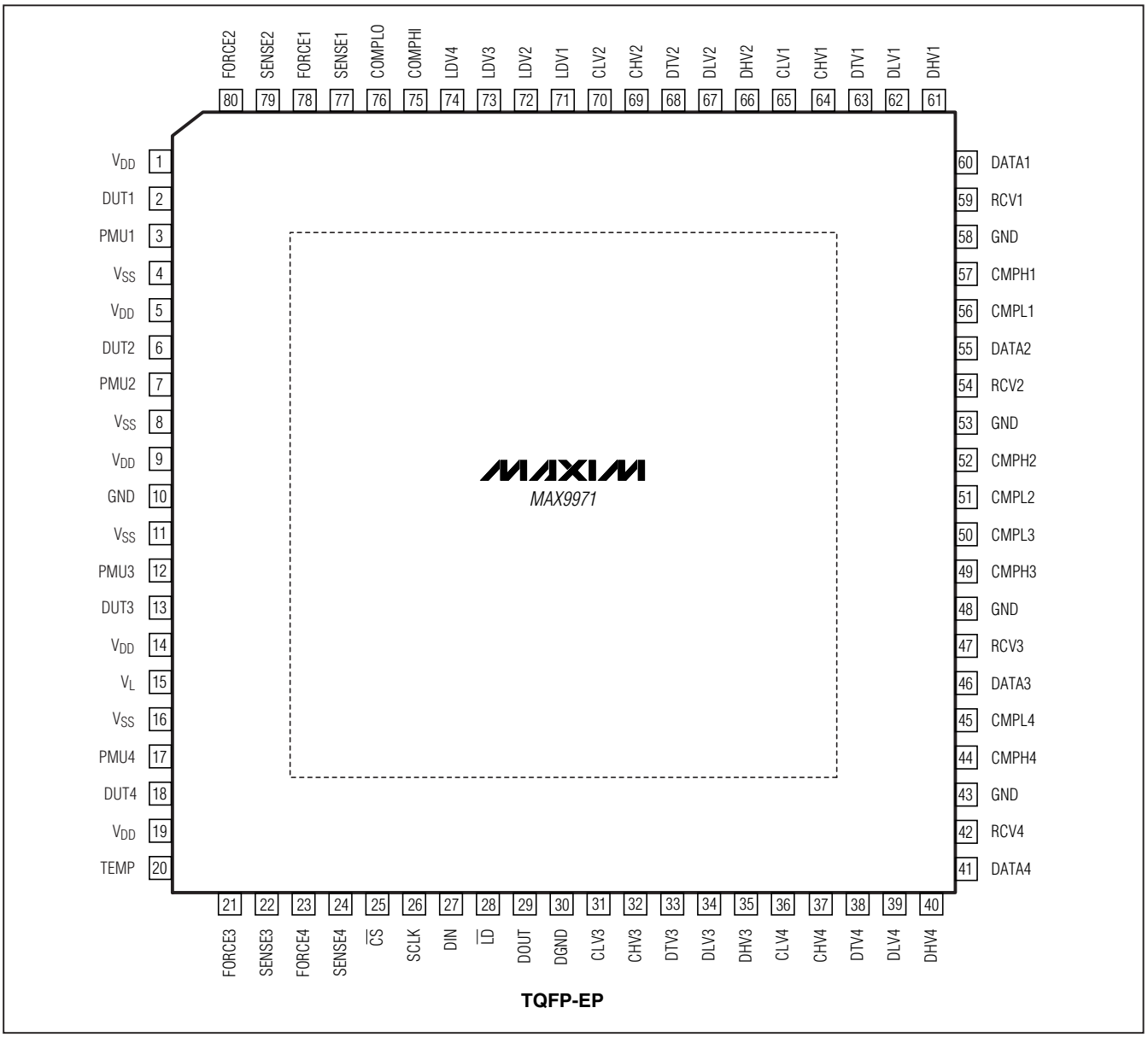
Pin Configurations (continued)



TQFP-EP

Chip Information

TRANSISTOR COUNT: 5728

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.